

# MJ21193 - PNP MJ21194 - NPN

## Silicon Power Transistors

The MJ21193 (PNP) and MJ21194 (NPN) utilize Perforated Emitter technology and are specifically designed for high power audio output, disk head positioners and linear applications.

### Features

- Total Harmonic Distortion Characterized
- High DC Current Gain
- Excellent Gain Linearity
- High SOA
- These Devices are Pb-Free and are RoHS Compliant\*

### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO}$	250	Vdc
Collector-Base Voltage	$V_{CBO}$	400	Vdc
Emitter-Base Voltage	$V_{EBO}$	5	Vdc
Collector-Emitter Voltage - 1.5 V	$V_{CEX}$	400	Vdc
Collector Current - Continuous	$I_C$	16	Adc
Collector Current - Peak (Note 1)	$I_{CM}$	30	Adc
Base Current - Continuous	$I_B$	5	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate Above $25^\circ\text{C}$	$P_D$	250 1.43	W W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +200	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Pulse Test: Pulse Width = 5  $\mu\text{s}$ , Duty Cycle  $\leq 10\%$ . (continued)

### THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.7	$^\circ\text{C}/\text{W}$

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

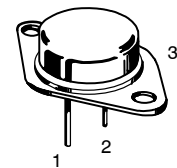
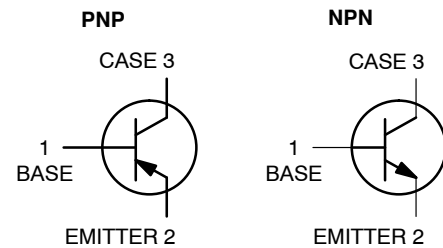


**ON Semiconductor®**

<http://onsemi.com>

## 16 AMP COMPLEMENTARY SILICON POWER TRANSISTORS 250 VOLTS, 250 WATTS

### SCHEMATIC



TO-204AA (TO-3)  
CASE 1-07  
STYLE 1

### MARKING DIAGRAM



MJ2119x = Device Code  
x = 3 or 4

G = Pb-Free Package  
A = Assembly Location  
YY = Year  
WW = Work Week  
MEX = Country of Origin

### ORDERING INFORMATION

Device	Package	Shipping†
MJ21193G	TO-3 (Pb-Free)	100 Units / Tray
MJ21194G	TO-3 (Pb-Free)	100 Units / Tray

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Collector–Emitter Sustaining Voltage (I <sub>C</sub> = 100 mA <sub>dc</sub> , I <sub>B</sub> = 0)	V <sub>CEO(sus)</sub>	250	–	–	V <sub>dc</sub>
Collector Cutoff Current (V <sub>CE</sub> = 200 V <sub>dc</sub> , I <sub>B</sub> = 0)	I <sub>CEO</sub>	–	–	100	μA <sub>dc</sub>
Emitter Cutoff Current (V <sub>CE</sub> = 5 V <sub>dc</sub> , I <sub>C</sub> = 0)	I <sub>EBO</sub>	–	–	100	μA <sub>dc</sub>
Collector Cutoff Current (V <sub>CE</sub> = 250 V <sub>dc</sub> , V <sub>BE(off)</sub> = 1.5 V <sub>dc</sub> )	I <sub>CEX</sub>	–	–	100	μA <sub>dc</sub>

### SECOND BREAKDOWN

Second Breakdown Collector Current with Base Forward Biased (V <sub>CE</sub> = 50 V <sub>dc</sub> , t = 1 s (non–repetitive) (V <sub>CE</sub> = 80 V <sub>dc</sub> , t = 1 s (non–repetitive))	I <sub>S/b</sub>	5 2.5	– –	– –	A <sub>dc</sub>
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### ON CHARACTERISTICS

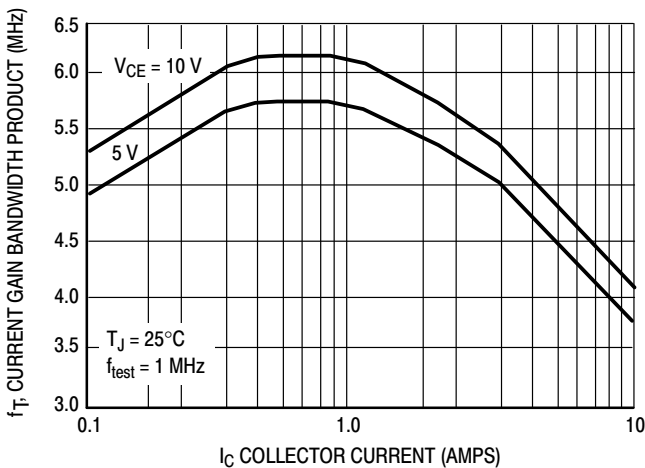
DC Current Gain (I <sub>C</sub> = 8 A <sub>dc</sub> , V <sub>CE</sub> = 5 V <sub>dc</sub> ) (I <sub>C</sub> = 16 A <sub>dc</sub> , I <sub>B</sub> = 5 A <sub>dc</sub> )	h <sub>FE</sub>	25 8	– –	75	
Base–Emitter On Voltage (I <sub>C</sub> = 8 A <sub>dc</sub> , V <sub>CE</sub> = 5 V <sub>dc</sub> )	V <sub>BE(on)</sub>	–	–	2.2	V <sub>dc</sub>
Collector–Emitter Saturation Voltage (I <sub>C</sub> = 8 A <sub>dc</sub> , I <sub>B</sub> = 0.8 A <sub>dc</sub> ) (I <sub>C</sub> = 16 A <sub>dc</sub> , I <sub>B</sub> = 3.2 A <sub>dc</sub> )	V <sub>CE(sat)</sub>	– –	– –	1.4 4	V <sub>dc</sub>

### DYNAMIC CHARACTERISTICS

Total Harmonic Distortion at the Output V <sub>RMS</sub> = 28.3 V, f = 1 kHz, P <sub>LOAD</sub> = 100 W <sub>RMS</sub> h <sub>FE</sub> (Matched pair h <sub>FE</sub> = 50 @ 5 A/5 V) h <sub>FE</sub> unmatched h <sub>FE</sub> matched	T <sub>HD</sub>	– –	0.8 0.08	– –	% %
Current Gain Bandwidth Product (I <sub>C</sub> = 1 A <sub>dc</sub> , V <sub>CE</sub> = 10 V <sub>dc</sub> , f <sub>test</sub> = 1 MHz)	f <sub>T</sub>	4	–	–	MHz
Output Capacitance (V <sub>CB</sub> = 10 V <sub>dc</sub> , I <sub>E</sub> = 0, f <sub>test</sub> = 1 MHz)	C <sub>ob</sub>	–	–	500	pF

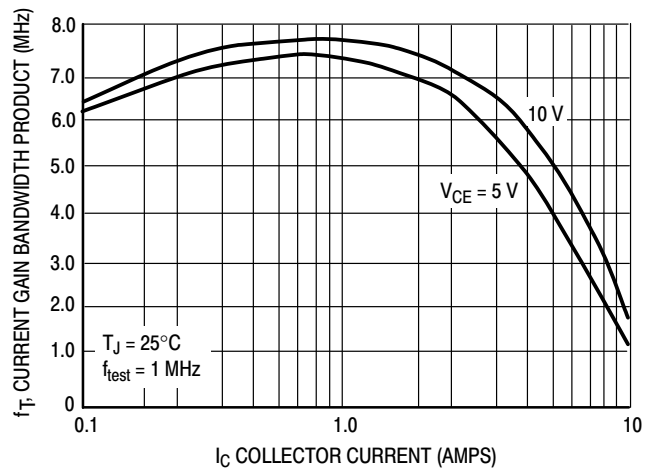
NOTE: Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤2%

**PNP MJ21193**



**Figure 1. Typical Current Gain Bandwidth Product**

**NPN MJ21194**



**Figure 2. Typical Current Gain Bandwidth Product**

TYPICAL CHARACTERISTICS

PNP MJ21193

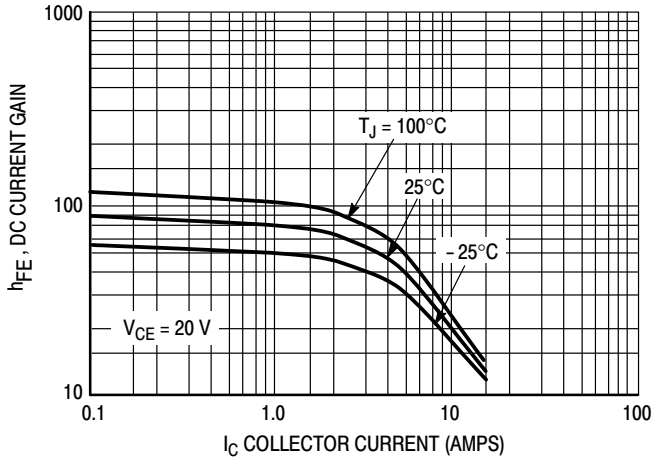


Figure 3. DC Current Gain,  $V_{CE} = 20\text{ V}$

NPN MJ21194

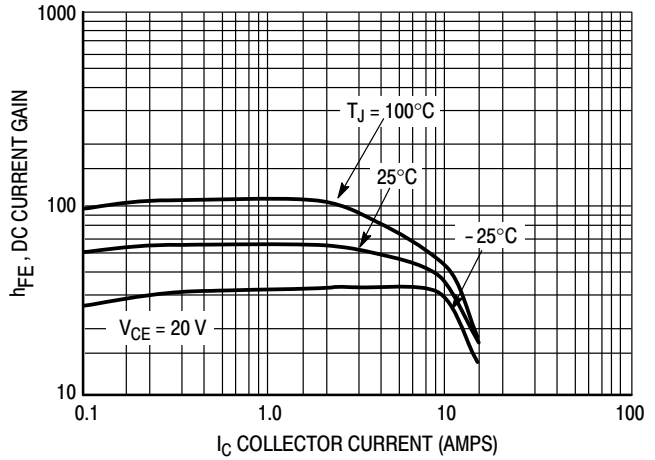


Figure 4. DC Current Gain,  $V_{CE} = 20\text{ V}$

PNP MJ21193

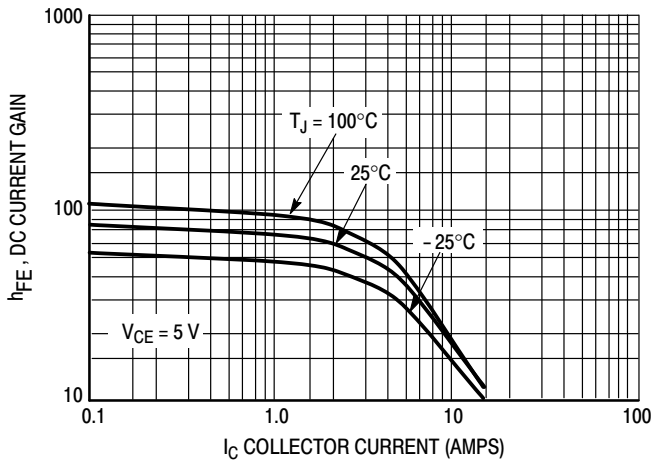


Figure 5. DC Current Gain,  $V_{CE} = 5\text{ V}$

NPN MJ21194

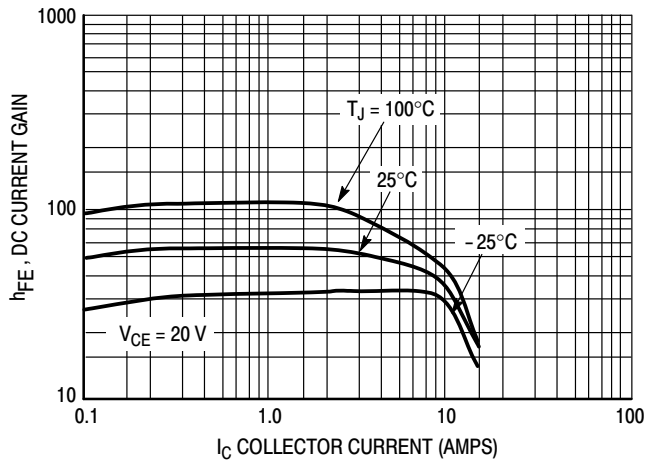


Figure 6. DC Current Gain,  $V_{CE} = 5\text{ V}$

PNP MJ21193

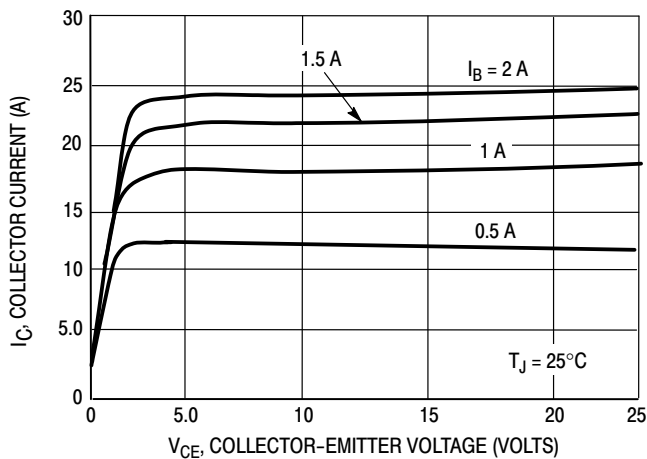


Figure 7. Typical Output Characteristics

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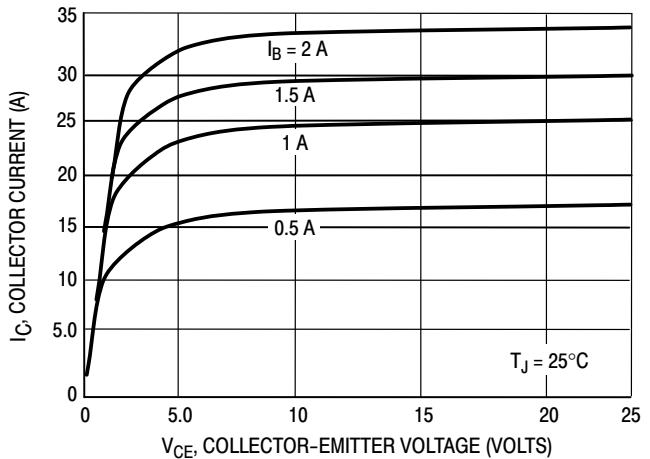


Figure 8. Typical Output Characteristics

TYPICAL CHARACTERISTICS

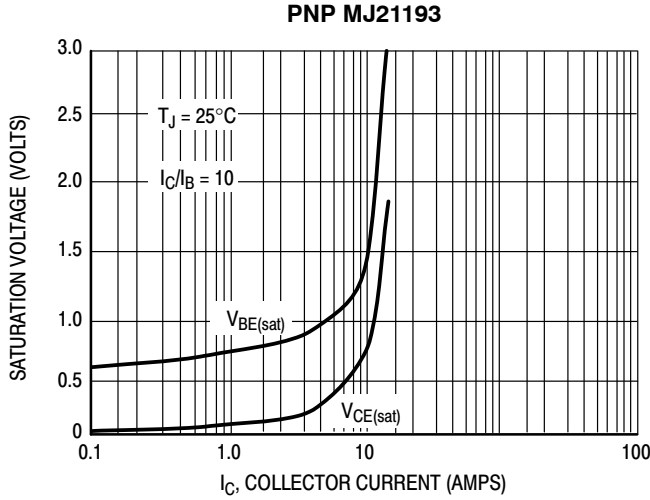


Figure 9. Typical Saturation Voltages

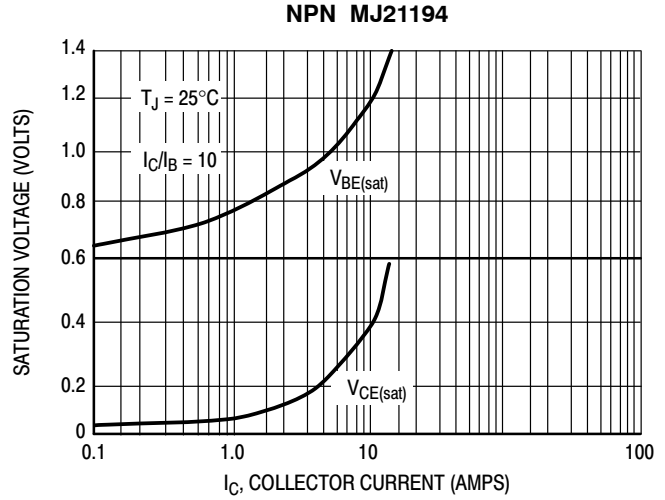


Figure 10. Typical Saturation Voltages

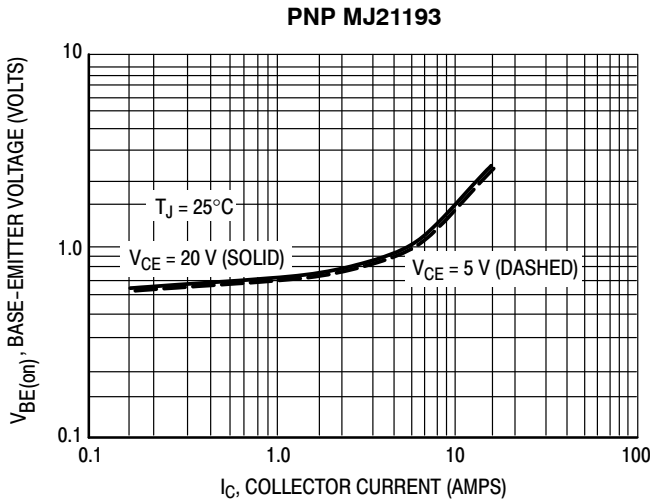


Figure 11. Typical Base-Emitter Voltage

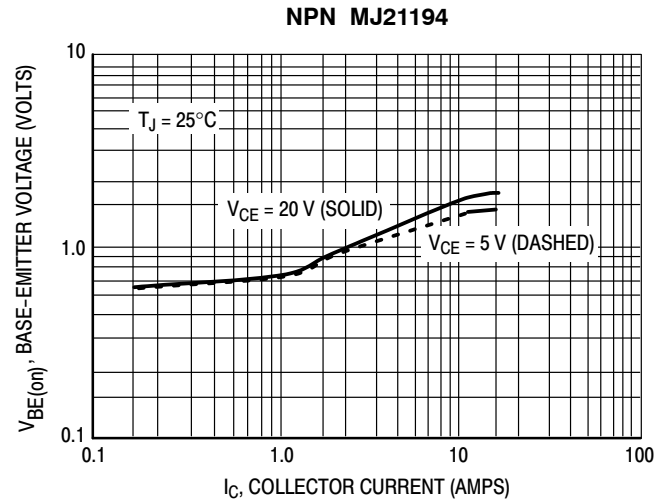


Figure 12. Typical Base-Emitter Voltage

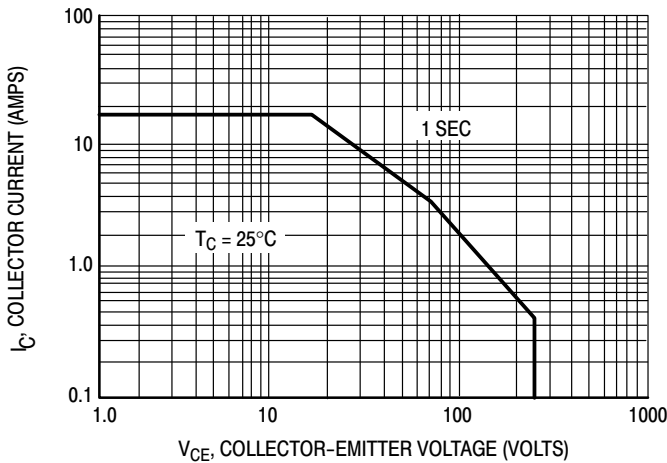


Figure 13. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on  $T_{J(pk)} = 200^\circ\text{C}$ ;  $T_C$  is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

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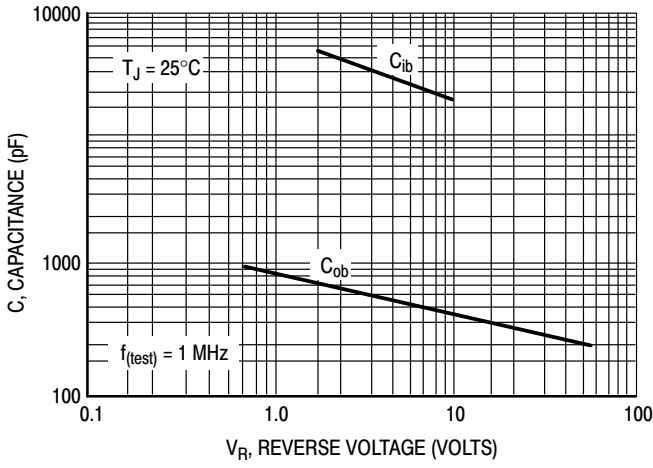


Figure 14. MJ21193 Typical Capacitance

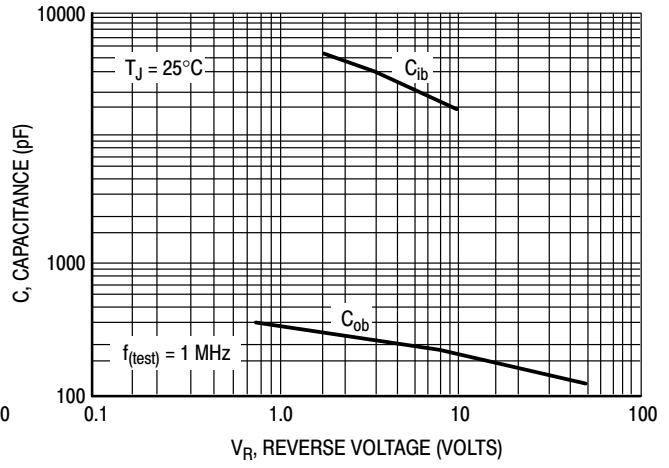


Figure 15. MJ21194 Typical Capacitance

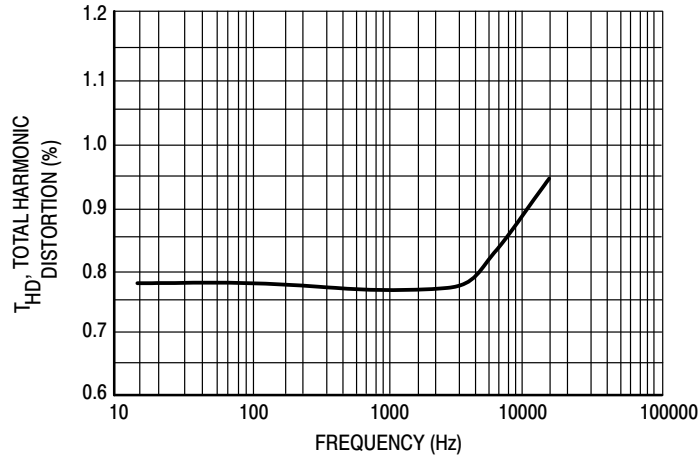


Figure 16. Typical Total Harmonic Distortion

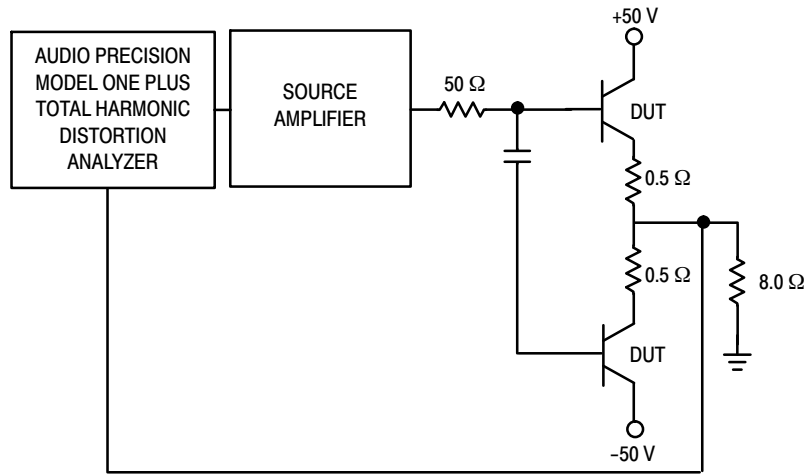
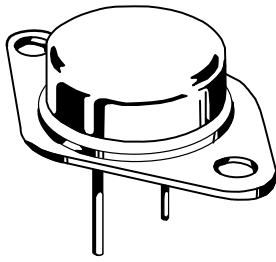


Figure 17. Total Harmonic Distortion Test Circuit

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor



TO-204 (TO-3)  
CASE 1-07  
ISSUE Z

DATE 05/18/1988

SCALE 1:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.550 REF	---	39.37 REF	---
B	---	1.050	---	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC	---	10.92 BSC	---
H	0.215 BSC	---	5.46 BSC	---
K	0.440	0.480	11.18	12.19
L	---	0.665 BSC	---	16.89 BSC
N	---	0.830	---	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC	---	30.15 BSC	---
V	0.131	0.188	3.33	4.77

- |                                                                    |                                                                    |                                                                         |                                                                       |                                                                               |
|--------------------------------------------------------------------|--------------------------------------------------------------------|-------------------------------------------------------------------------|-----------------------------------------------------------------------|-------------------------------------------------------------------------------|
| <p>STYLE 1:<br/>PIN 1. BASE<br/>2. EMITTER<br/>CASE: COLLECTOR</p> | <p>STYLE 2:<br/>PIN 1. BASE<br/>2. COLLECTOR<br/>CASE: EMITTER</p> | <p>STYLE 3:<br/>PIN 1. GATE<br/>2. SOURCE<br/>CASE: DRAIN</p>           | <p>STYLE 4:<br/>PIN 1. GROUND<br/>2. INPUT<br/>CASE: OUTPUT</p>       | <p>STYLE 5:<br/>PIN 1. CATHODE<br/>2. EXTERNAL TRIP/DELAY<br/>CASE: ANODE</p> |
| <p>STYLE 6:<br/>PIN 1. GATE<br/>2. EMITTER<br/>CASE: COLLECTOR</p> | <p>STYLE 7:<br/>PIN 1. ANODE<br/>2. OPEN<br/>CASE: CATHODE</p>     | <p>STYLE 8:<br/>PIN 1. CATHODE #1<br/>2. CATHODE #2<br/>CASE: ANODE</p> | <p>STYLE 9:<br/>PIN 1. ANODE #1<br/>2. ANODE #2<br/>CASE: CATHODE</p> |                                                                               |

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