

M5201L, P, FP**GENERAL PURPOSE SWITCHING OPERATIONAL AMPLIFIER
(DUAL INPUT, SINGLE OUTPUT TYPE)**

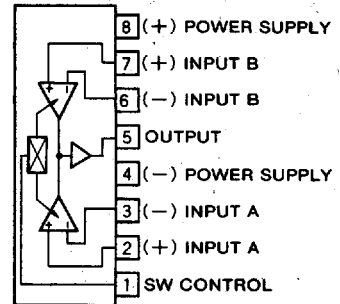
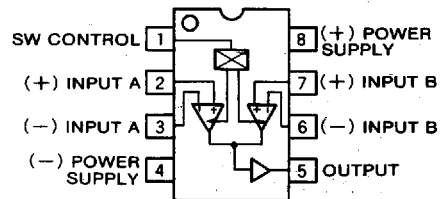
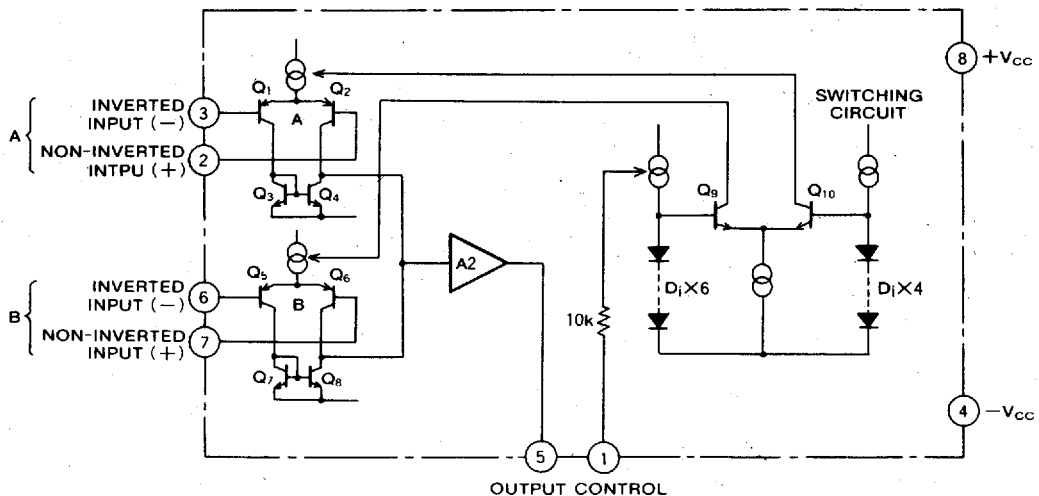
MITSUBISHI ELEK (LINEAR) 53E D ■ 6249826 0014044 511 ■ MIT2

DESCRIPTION

The M5201 is a semiconductor integrated circuit designed for an operational amplifier which adopts analog switch function, having dual inputs of A and B and a single output. The device comes in an 8-pin SIP, DIP or FP and contains input differential circuits of A and B type, single output circuit and a switching circuit of an operational amplifier, and can be used as a conventional operational amplifier, turning on A or B inputs by externally setting the control pin at high or low level. For a voltage follower condition where $G_V = 0\text{dB}$, the device functions merely as an analog switch, but, for an amplifier with a switching function, gain can be set independently for A and B inputs. The M5201 operational amplifier has basic characteristics similar to those of the M5218/M5R4558P and can be widely used as audio, video and musical instrument equipments.

FEATURES

- Operational amplifier inputs of A and B type and gain can be set independently
- Applicable to both single and dual power supplies
- High gain, low distortion
..... $G_{VO} = 100\text{dB}$, $\text{THD} = 0.002\%$ (typ.)
- High slew rate, high f_T $\text{SR} = 2.2\text{V}/\mu\text{s}$, $f_T = 7\text{MHz}$ (typ.)
- Low noise ($R_S = 1\text{k}\Omega$) FLAT $V_{NI} = 2\mu\text{Vrms}$ (typ.)
- Small switching shock noise
- High load current, high power dissipation
..... $I_{LP} = \pm 50\text{mA}$, $P_d = 800\text{mW}$ (SIP)
..... $P_d = 625\text{mW}$ (DIP)
..... $P_d = 440\text{mW}$ (FP)

PIN CONFIGURATION (TOP VIEW)**Outline 8P5 (M5201L)****Outline 8P4 (M5201P)
8P2S (M5201FP)****RECOMMENDED OPERATING CONDITIONS**Supply voltage range $\pm 2.5 \sim \pm 16\text{V}$ Rated supply voltage $\pm 15\text{V}$ **EQUIVALENT CIRCUIT**

M5201L. P. FP

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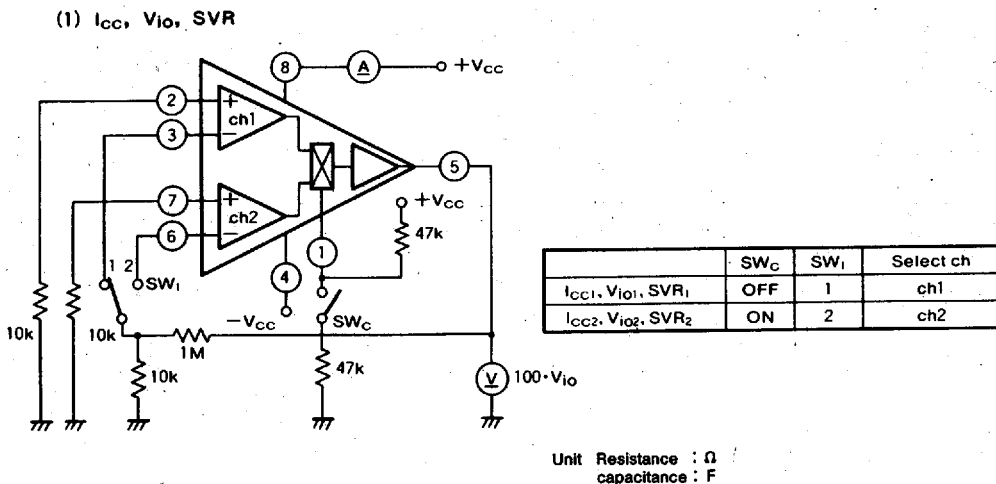
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Ratings	Unit
V_{CC}	Supply voltage	$\pm 18(36)$	V
V_{id}	Differential input voltage	± 30	V
V_{ic}	Common phase input voltage	± 15	V
I_{LP}	Load current	± 50	mA
P_d	Power dissipation	800(SIP)/625(DIP)/440(FP)	mW
T_{opr}	Ambient temperature	$-20 \sim +75$	$^{\circ}\text{C}$
T_{stg}	Storage temperature	$-55 \sim +125$	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS ($V_{CC} = \pm 15\text{V}$)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{CC}	Circuit current	V_{in} SW ON		2.3	6.0	mA
		SW OFF		2.1	6.0	
V_{IO}	Input offset voltage	$R_s = 10\text{k}\Omega$		0.8	6.0	mV
I_B	Input bias current			80	500	nA
G_{VO}	Open loop voltage gain	$R_L = 2\text{k}\Omega$		100		dB
V_{OM}	Maximum output voltage	$R_L \geq 10\text{k}\Omega$	± 12	± 14		V
THD	Total harmonic distortion	$f = 1\text{kHz}, V_o = 5\text{Vrms}, G_v = 20\text{dB}$		0.002		%
SVR	Supply voltage rejection ratio			20	150	$\mu\text{V/V}$
C·S	Channel separation	$f = 1\text{kHz}$		82		dB
f_T	Gain bandwidth product	$G_v = 0\text{dB}$		7		MHz
SR	Slew rate	$G_v = 0\text{dB}, R_L = 2\text{k}\Omega // 100\text{pF}$		2.2		$\text{V}/\mu\text{s}$
V_{NI}	Input referred noise voltage	$R_s = 1\text{k}\Omega, \text{BW} = 10\text{Hz} \sim 30\text{kHz}, \text{Flat}$		2.0		μVrms

TEST CIRCUIT

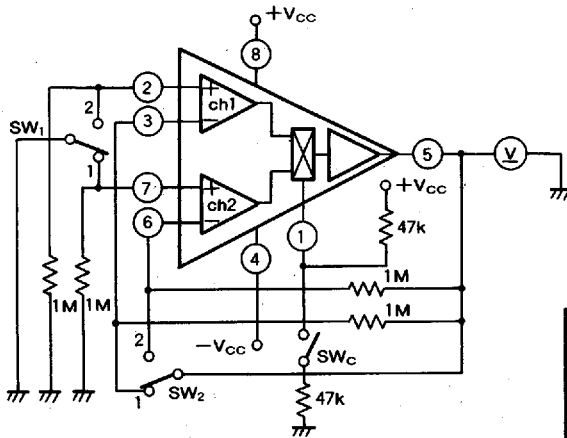


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(2) I_b , I_{io}



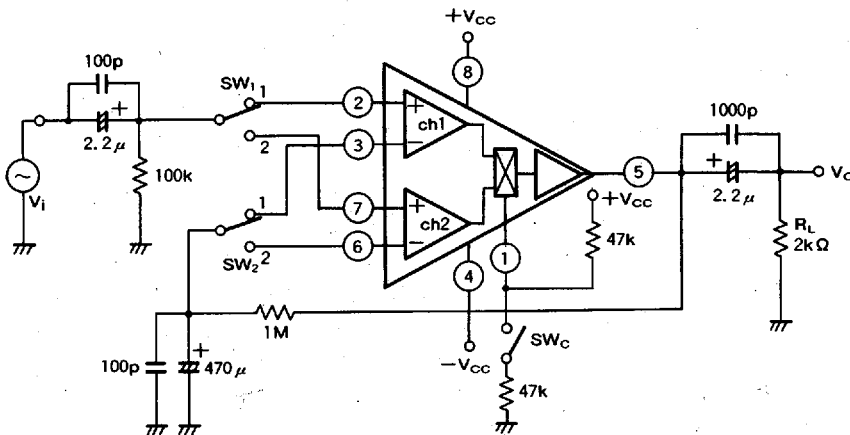
$$I_b^+ = V_{O1} / 1M\Omega$$

$$I_b^- = V_{O2} / 1M\Omega$$

$$I_{io} = |I_b^+ - I_b^-|$$

	SW _C	SW ₁	SW ₂	Select ch
V _{O1}	OFF	1	1	ch1
V _{O1}	OFF	2	2	ch1
V _{O2}	ON	2	2	ch2
V _{O2}	ON	1	1	ch2

(3) f_t , G_v



	SW _C	SW ₁	SW ₂	Select ch
f_{t1} , G_{v1}	OFF	1	1	ch1
f_{t2} , G_{v2}	ON	2	2	ch2

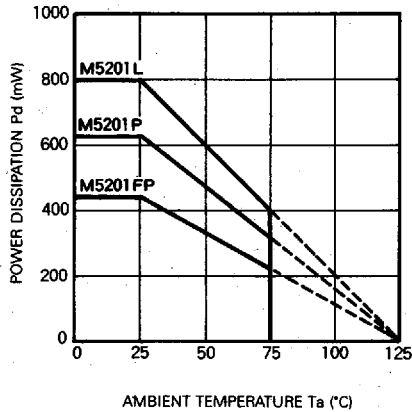
Unit Resistance: Ω
Capacitance: F

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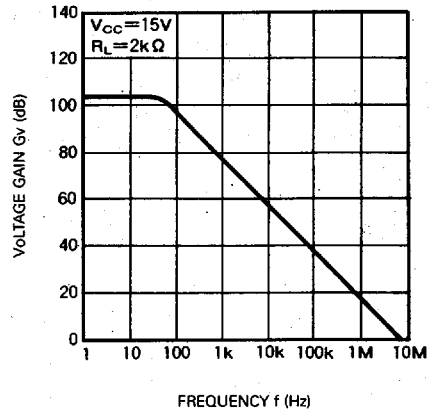
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TYPICAL CHARACTERISTICS

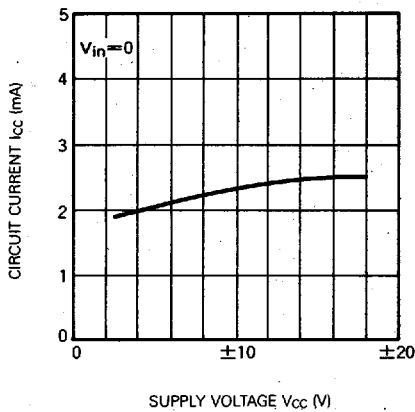
THERMAL DERATING (MAXIMUM RATING)



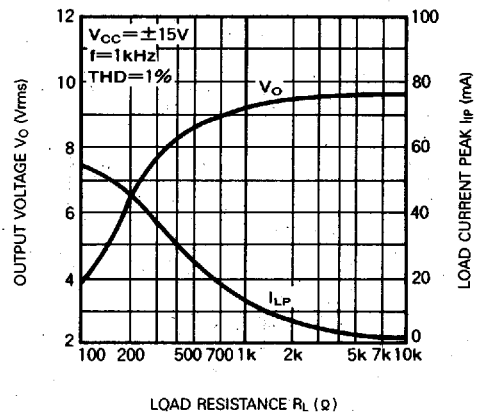
VOLTAGE GAIN VS. FREQUENCY RESPONSE



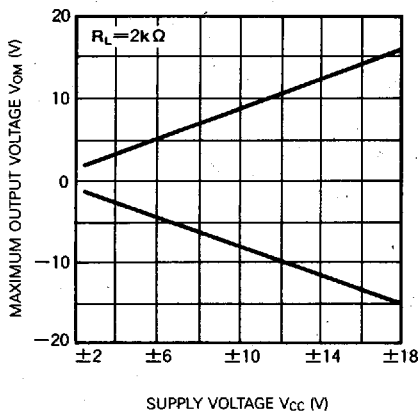
CIRCUIT CURRENT VS. SUPPLY VOLTAGE



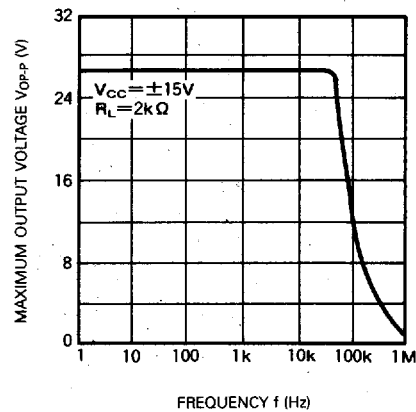
OUTPUT VOLTAGE/LOAD CURRENT PEAK VS. LOAD RESISTANCE



MAXIMUM OUTPUT VOLTAGE VS. SUPPLY VOLTAGE



MAXIMUM OUTPUT VOLTAGE VS. FREQUENCY RESPONSE

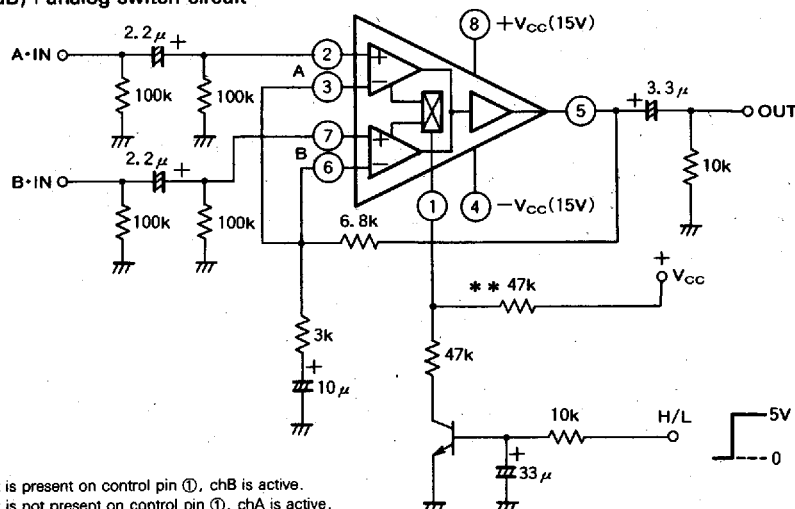


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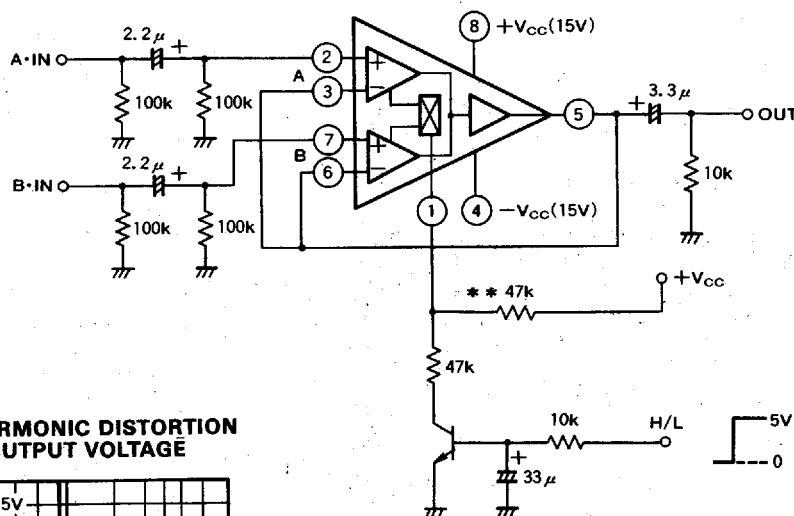
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APPLICATION CIRCUIT

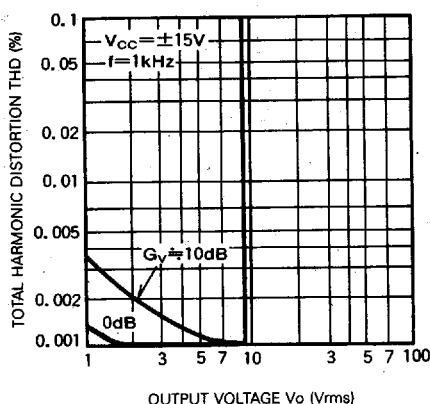
(1) FLAT amplifier ($G_v \approx 10\text{dB}$) + analog switch circuit



(2) Analog switch circuit ($D_v = 0\text{dB}$, voltage follower amplifier)



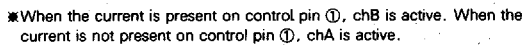
**TOTAL HARMONIC DISTORTION
 VS. OUTPUT VOLTAGE**



A resistor indicated by ** is a pull-up resistor to prevent switching pin ① from being activated by the leak current from an external circuit (i.e. TR).

**MITSUBISHI ELEK (LINEAR)
TYPICAL APPLICATION CIRCUIT**

53E D ■ 6249826 0014049 0T3 ■ MIT2



Unit Resistance: Ω
Capacitance: F

WIRING ON THE PCB

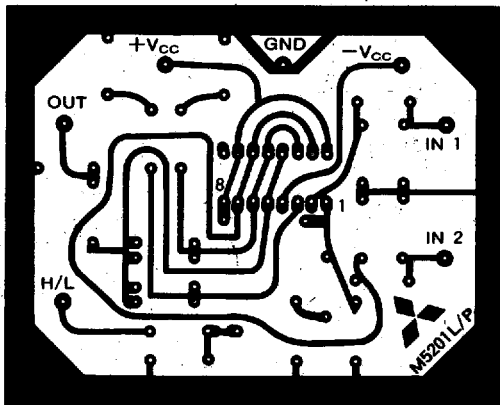


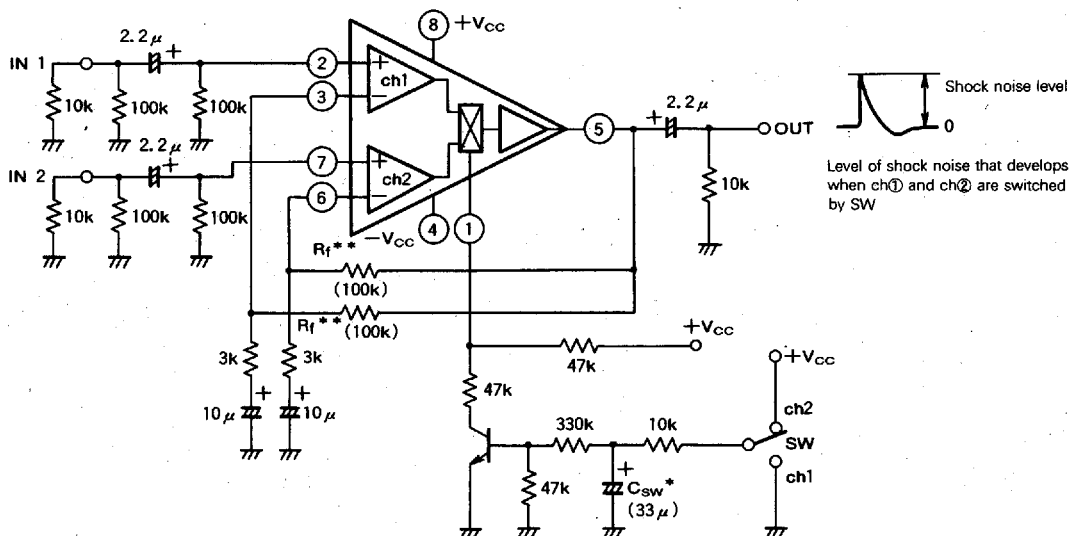
Diagram of a 2SC2603 transistor circuit. The circuit includes two input channels, IN 1 and IN 2, each with a 2.2μF coupling capacitor and a 100kΩ resistor to ground. The transistor is a 2SC2603, with a 47kΩ base resistor and a 0.0022μF bypass capacitor. The output is taken from the collector through a 33μF capacitor and a 10kΩ resistor. The circuit is powered by a +VCC supply and has a GND connection. A note indicates the circuit is applicable for SIP and DIP packages.

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53E D

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TEST CIRCUIT



Graph showing Shock Noise (mV) versus Capacitor C_{sw} (μF) for $V_{cc} = \pm 15V$ and $G_v = 30dB$. The noise is relatively flat around 200 mV for C_{sw} between 0.01 and 10 μF , then decreases to about 140 mV at 100 μF .

* Characteristic of shock noise with respect to change of C_{sw}

Graph showing Shock Noise (V) versus Voltage Gain G_v (dB) for the AD633. The y-axis is logarithmic, ranging from 0.01 to 1.0 V. The x-axis is linear, ranging from 0 to 40 dB. The curve shows that shock noise increases with voltage gain. Operating conditions: $V_{CC} = \pm 15V$, $C_{SW} = 33 \mu F$.

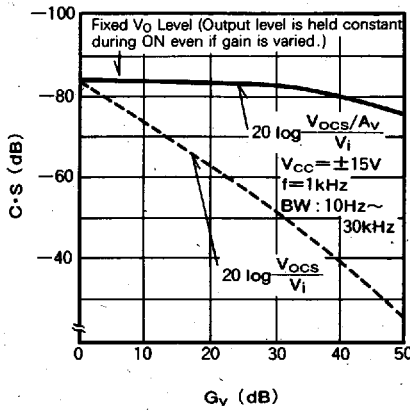
Voltage Gain G_v (dB)	Shock Noise (V)
0	0.012
10	0.025
20	0.050
30	0.150
40	1.000

* * Characteristic of shock noise with respect to voltage gain varied by R1.

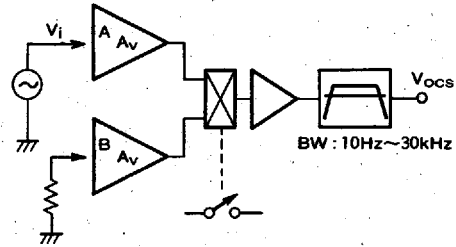
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CHANNEL SEPARATION (C-S)



(A:OFF/B:IN ON MODE)



$$C \cdot S = 20 \log \left[\frac{\text{INPUT LEAK LEVEL}}{\text{SIGNAL LEVEL}} \right] \text{ (dB)}$$

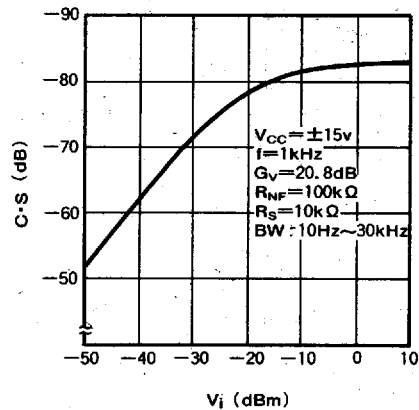
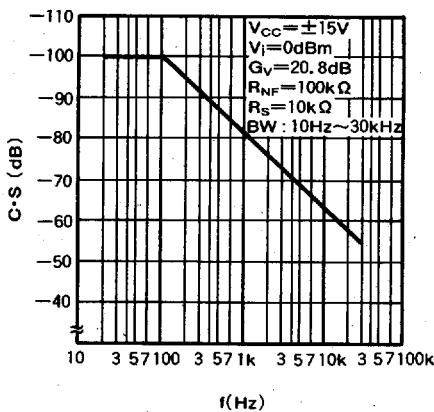
$$= 20 \log \frac{V_{OCS}/A_v}{V_i} \text{ (dB)}$$

Channel separation is defined as the ratio of the leak signal (that is scaled on the assumption it is present in the input) to the input signal.

$$\left(20 \log \frac{V_{OCS}/A_v}{V_i} \right)$$

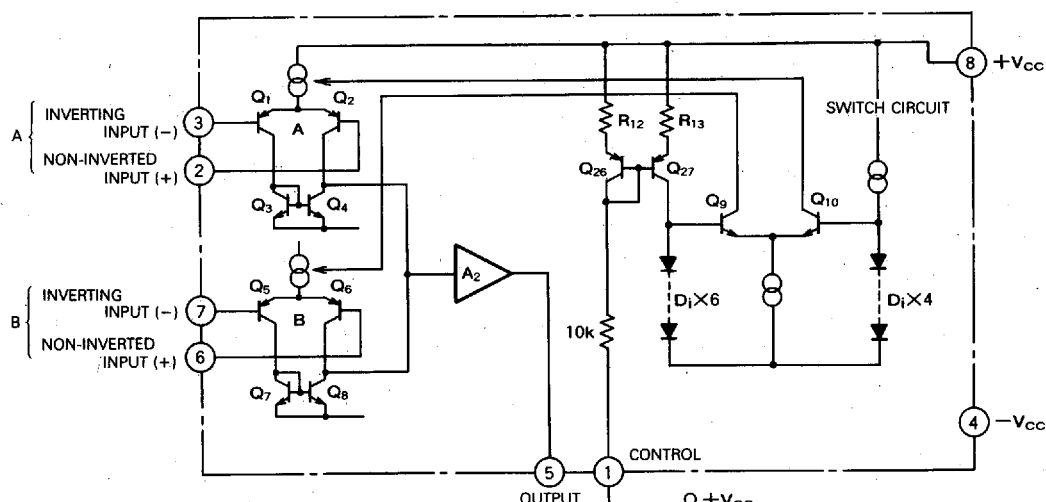
However, as indicated by the above broken line, if gain (A_v) is not scaled, channel separation appears to be deteriorated by as much as the amplified amount.

$$\left(20 \log \frac{V_{OCS}}{V_i} \right)$$



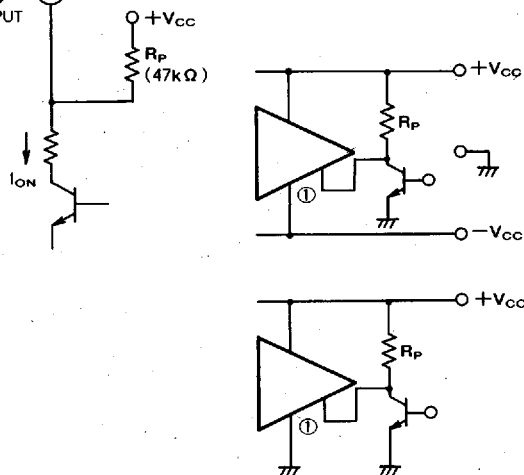
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SWITCHING MECHANISM

As shown in the above figure, the M5201 transfers switching signals by externally feeding the current to the V_F on the Q_{26} side of the current mirror transistor circuit (which consists of transistors Q_{26} and Q_{27}). That is, when no current is fed to pin ①, Q_{10} is turned on by four diodes connected to Q_{10} to activate the amplifier for channel A. When current is fed to pin ①, the collector current to Q_9 flows to turn on the six diodes connected to Q_9 and channel B is activated. Thus, applying or removing current to/from pin ① switches an active channel, therefore, M5203 can arbitrarily control the driving method regardless of the type of power supply (single or dual).

It is recommended to connect a pull-up resistor R_P to pin ① to reduce the current sensitivity of transistor Q_{26} because a very small current may turn on the V_F .



PIN (1) TURN-ON CURRENT WHEN A PULL-UP RESISTOR R_P IS CONNECTED I_{ON} ($R_P = 47k\Omega$)

