NJM4560

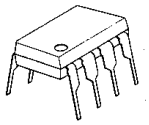
The 4560 integrated circuit is a high-gain, wide-bandwidth, dual operational amplifier capable of driving 20V peak-to-peak into 400Ω loads. The 4560 combines many of the features of the 4558 as well as providing the capability of wider bandwidth, and higher slew rate make the 4560 ideal for active filters, data and telecommunications, and many instrumentation applications. The availability of the 4560 in the surface mounted micro-package allows the 4560 to be used in critical applications requiring very high packing densities.

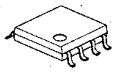
■ Absolute Maximum Ratings (Ta=25°C)

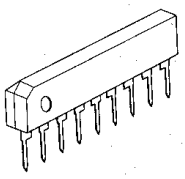
Supply Voltage	V^+/V^-	±18V
Differential Input Voltage	V_{ID}	±30V
Input Voltage (note)	V_I	±15V
Power Dissipation	P_D (D,S,T-Type)	500mW
	(M,E-Type)	300mW
Operating Temperature Range	T_{opr}	−20~+ 75°C
Storage Temperature Range	T_{stg}	−40~+125°C

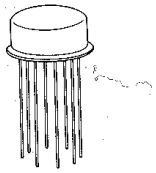
(note) For supply voltage less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

■ Package Outline


NJM4560D


NJM4560M
NJM4500E

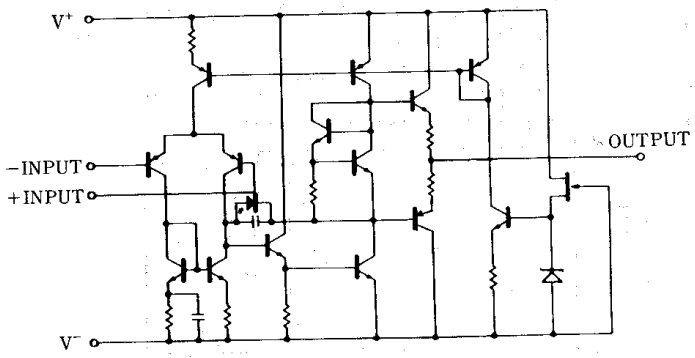

NJM4560S


NJM4560T

■ Electrical Characteristics (T_a=25°C, V^+=15V, V^-=−15V)

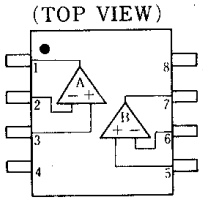
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Input Offset Voltage	V_{IO}	R_S≦10kΩ	—	0.5	6	mV
Input Offset Current	I_{IO}		—	10	200	nA
Input Bias Current	I_{IB}		—	40	500	nA
Input Resistance	R_{IN}		0.3	5	—	MΩ
Large Signal Voltage Gain	A_V	R_L≧2kΩ, V_O=±10V	20	100	—	$\times 10^3$
Maximum Output Voltage	V_{OM}	R_L≧2kΩ	±12	±14	—	V
Maximum Output Voltage	V_{OM}	I_O=25mA	±10	±11.5	—	V
Input Common Mode Voltage Range	V_{ICM}		±12	±14	—	V
Common Mode Rejection Ratio	CMR	R_S≦10kΩ	70	90	—	dB
Supply Voltage Rejection Ratio	SVR	R_S≦10kΩ	—	30	150	μV/V
Power Dissipation	P_D		—	105	170	mW
Slew Rate	SR	R_L≧2kΩ	—	4	—	V/μs
Unity Gain Bandwidth	f_T		—	10	—	MHz

■ Equivalent Circuit (½ Shown)

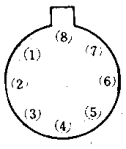


■ Connection Diagram

D.M.E Type (TOP VIEW)

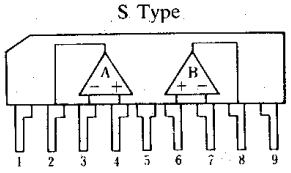


T Type (TOP VIEW)



PIN FUNCTION
1. A OUTPUT
2. A−INPUT
3. A+INPUT
4. V⁻
5. B+INPUT
6. B−INPUT
7. B OUTPUT
8. V⁺

S Type



PIN FUNCITON
1. V⁺
2. A OUTPUT
3. A−INPUT
4. A+INPUT
5. V⁻
6. B+INPUT
7. B−INPUT
8. B OUTPUT
9. V⁺