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# NTE74LS93
# Integrated Circuit
# TTL – 4–Bit Binary Counter

**Description:**

The NTE74LS93 is a monolithic 4–bit binary counter in a 14–Lead DIP type package that contains four master–slave flip–flops and additional gating to provide a divide–by–two counter and a three–stage binary counter for which the count cycle length is divide–by–eight. The counter also contains a gated zero reset.

To use the maximum count length of this device, the CKB input is connected to the $Q_A$ output. The input count pulses are applied to CKA input and the outputs are as described in the function tables.

**Absolute Maximum Ratings:** (Note 1)

Supply Voltage, $V_{CC}$ . . . . . 7V
Input Voltage, $V_{IN}$
R Inputs . . . . . 7V
A and B Inputs . . . . . 5.5V
Power Dissipation . . . . . 45mW
Operating Temperature Range, $T_A$ . . . . . 0°C to +70°C
Storage Temperature Range, $T_{stg}$ . . . . . –65°C to +150°C

Note 1. Unless otherwise specified, all voltages are referenced to GND.

**Recommended Operating Conditions:**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage | $V_{CC}$ | 4.75 | 5.0 | 5.25 | V |
| High–Level Output Current | $I_{OH}$ | – | – | –400 | μA |
| Low–Level Output Current | $I_{OL}$ | – | – | 8 | mA |
| Count Frequency<br>A Input | $f_{count}$ | 0 | – | 32 | MHz |
| B Input | | 0 | – | 16 | MHz |
| Pulse Width<br>A Input | $t_w$ | 15 | – | – | ns |
| B Input | | 30 | – | – | ns |
| Reset Inputs | | 30 | – | – | ns |
| Reset Inactive Setup Time | $t_{su}$ | 25 | – | – | ns |
| Operating Temperature Range | $T_A$ | 0 | – | +70 | °C |

**Electrical Characteristics:** (Note 2, Note 3)

| Parameter | Symbol | Test Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| High−Level Input Voltage | $V_{IH}$ | | | 2 | – | – | V |
| Low−Level Input Voltage | $V_{IL}$ | | | – | – | 0.8 | V |
| Input Clamp Voltage | $V_{IK}$ | $V_{CC}$ = MIN, $I_I$ = −18mA | | – | – | −1.5 | V |
| High Level Output Voltage | $V_{OH}$ | $V_{CC}$ = MIN, $V_{IH}$ = 2V, $V_{IL}$ = MAX, $I_{OH}$ = −400μA | | 2.7 | 3.4 | – | V |
| Low Level Output Voltage | $V_{OL}$ | $V_{CC}$ = MIN, $V_{IH}$ = 2V, $V_{IL}$ = MAX, Note 4 | $I_{OL}$ = 4mA | – | 0.25 | 0.4 | V |
| | | | $I_{OL}$ = 8mA | – | 0.35 | 0.5 | V |
| Input Current | $I_I$ | $V_{CC}$ = MAX, $V_I$ = 7V, Any Reset | | – | – | 0.1 | mA |
| | | $V_{CC}$ = MAX, $V_I$ = 5.5V | CKA or CKB | – | – | 0.2 | mA |
| High Level Input Current | $I_{IH}$ | $V_{CC}$ = MAX, $V_I$ = 2.7V | Any Reset | – | – | 20 | μA |
| | | | CKA or CKB | – | – | 80 | μA |
| Low Level Input Current | $I_{IL}$ | $V_{CC}$ = MAX, $V_I$ = 0.4V | Any Reset | – | – | −0.4 | mA |
| | | | CKA | – | – | −2.4 | mA |
| | | | CKB | – | – | −1.6 | mA |
| Short−Circuit Output Current | $I_{OS}$ | $V_{CC}$ = MAX, Note 5 | | −20 | – | −100 | mA |
| Supply Current | $I_{CC}$ | $V_{CC}$ = MAX, Note 6 | | – | 9 | 15 | mA |

Note 2. .For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.

Note 3. All typical values are at $V_{CC}$ = 5V, $T_A$ = +25°C.

Note 4. $Q_A$ outputs are tested at specified $I_{OL}$ plus the limit value of $I_{IL}$ for the CKB input. This permits driving the CKB input while maintaining full fan−out capability.

Note 5. Not more than one output should be shorted at a time and duration of short−circuit should not exceed one second.

Note 6. $I_{CC}$ is measured with all outputs open, both $R_O$ inputs grounded following momentary connection to 4.5V, and all other inputs grounded.

**Switching Characteristics:** ($V_{CC}$ = 5V, $T_A$ = +25°C unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Maximum Count Frequency (From CKA Input to $Q_A$ Output) | $f_{max}$ | $R_L$ = 2kΩ, $C_L$ = 15pF | 32 | 42 | – | MHz |
| (From CKB Input to $Q_B$ Output) | | | 16 | – | – | MHz |
| Propagation Delay Time (From CKA Input to $Q_A$ Output) | $t_{PLH}$ | | – | 10 | 16 | ns |
| | $t_{PHL}$ | | – | 12 | 18 | ns |
| Propagation Delay Time (From CKA Input to $Q_D$ Output) | $t_{PLH}$ | | – | 46 | 70 | ns |
| | $t_{PHL}$ | | – | 46 | 70 | ns |
| Propagation Delay Time (From CKB Input to $Q_B$ Output) | $t_{PLH}$ | | – | 10 | 16 | ns |
| | $t_{PHL}$ | | – | 14 | 21 | ns |
| Propagation Delay Time (From CKB Input to $Q_C$ Output) | $t_{PLH}$ | | – | 21 | 32 | ns |
| | $t_{PHL}$ | | – | 23 | 35 | ns |
| Propagation Delay Time (From CKB Input to $Q_D$ Output) | $t_{PLH}$ | | – | 34 | 51 | ns |
| | $t_{PHL}$ | | – | 34 | 51 | ns |
| Propagation Delay Time (From Set−to−0 Input to Any Output) | $t_{PHL}$ | | – | 26 | 40 | ns |

## Count Sequence (NOTE):

| Count | Outputs | | | |
|---|---|---|---|---|
| | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| 0 | L | L | L | L |
| 1 | L | L | L | H |
| 2 | L | L | H | L |
| 3 | L | L | H | H |
| 4 | L | H | L | L |
| 5 | L | H | L | H |
| 6 | L | H | H | L |
| 7 | L | H | H | H |
| 8 | H | L | L | L |
| 9 | H | L | L | H |
| 10 | H | L | H | L |
| 11 | H | L | H | H |
| 12 | H | H | L | L |
| 13 | H | H | L | H |
| 14 | H | H | H | L |
| 15 | H | H | H | H |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Irrelevant
NOTE: Output $Q_A$ is connected to input CKB.

## Reset/Count Function Table:

| Reset Inputs | | Outputs | | | |
|---|---|---|---|---|---|
| $R_{0(1)}$ | $R_{0(2)}$ | $Q_D$ | $Q_C$ | $Q_B$ | $Q_A$ |
| H | H | L | L | L | L |
| L | X | Count | | | |
| X | L | Count | | | |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Irrelevant

**Pin Connection Diagram**