MJW21192 (NPN), MJW21191 (PNP)

Complementary Silicon Plastic Power Transistors

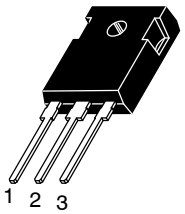
Specifically designed for power audio output, or high power drivers in audio amplifiers.

- DC Current Gain Specified up to 8.0 A at Temperature
- All On Characteristics at Temperature
- High SOA: 20 A, 18 V, 100 ms
- TO−247AE Package
- Pb−Free Packages are Available*

ON Semiconductor®

http://onsemi.com

8.0 A
POWER TRANSISTORS
COMPLEMENTARY SILICON
150 V, 125 W



TO−247
CASE 340L
STYLE 3

MAXIMUM RATINGS

Rating	Symbol	MJW21191 MJW21192	Unit
Collector−Emitter Voltage	V_{CEO}	150	Vdc
Collector−Base Voltage	V_{CB}	150	Vdc
Emitter−Base Voltage	V_{EB}	5.0	Vdc
Collector Current − Continuous − Peak	I_C	8.0 16	Adc
Base Current	I_B	2.0	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 0.65	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.0	°C/W
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	50	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

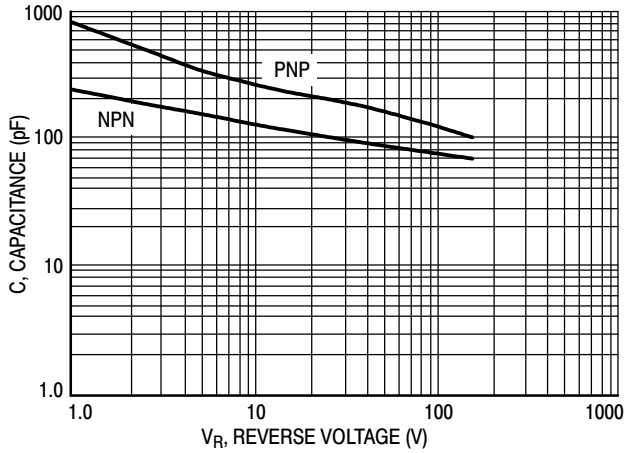
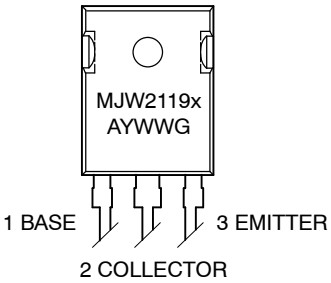


Figure 1. Typical Capacitance @ 25°C

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MARKING DIAGRAM



x = 1 or 2
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping
MJW21191	TO−247	30 Units/Rail
MJW21191G	TO−247 (Pb−Free)	30 Units/Rail
MJW21192	TO−247	30 Units/Rail
MJW21192G	TO−247 (Pb−Free)	30 Units/Rail

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Sustaining Voltage (Note 1) (I_C = 10 mAdc, I_B = 0)	$V_{CEO(sus)}$	150	–	Vdc
Collector Cutoff Current (V_{CB} = 250 Vdc, I_E = 0)	I_{CES}	–	10	μAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	10	μAdc
ON CHARACTERISTICS (Note 1)				
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 2.0 Vdc) (I_C = 8.0 Adc, V_{CE} = 2.0 Vdc)	h_{FE}	15 5.0	100 –	–
Collector−Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 0.4 Adc) (I_C = 8.0 Adc, I_B = 1.6 Adc)	$V_{CE(sat)}$	– –	1.0 2.0	Vdc
Base−Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$	–	2.0	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain − Bandwidth Product (Note 2) (I_C = 1.0 Adc, V_{CE} = 10 Vdc, f_{test} = 1.0 MHz)	f_T	4.0	–	MHz

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
2. $f_T = |h_{fe}| \bullet f_{test}$.

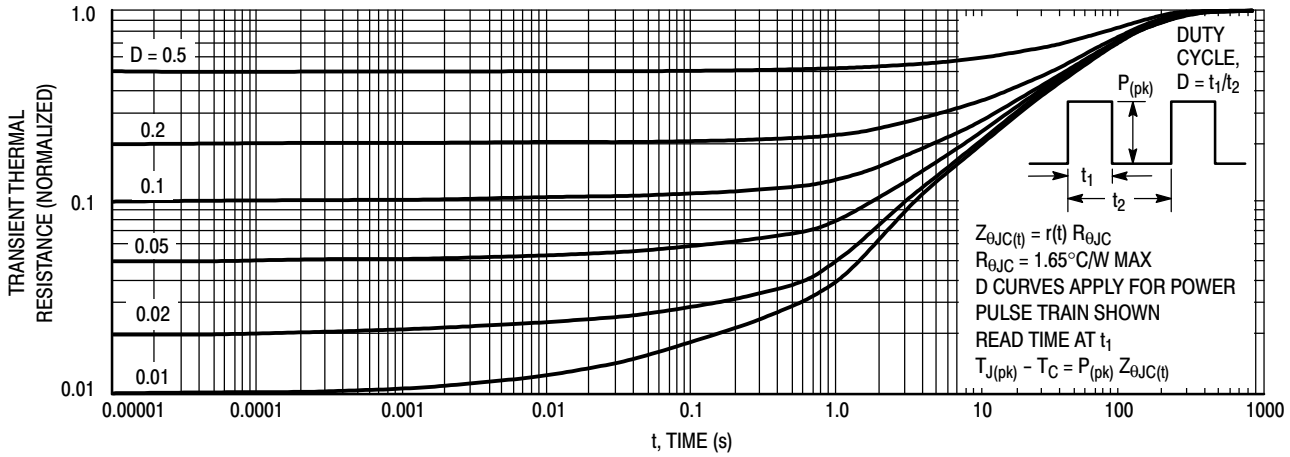


Figure 2. Thermal Response

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation then the curves indicate.

The data of Figures 3 and 4 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 2. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

NPN — MJW21192

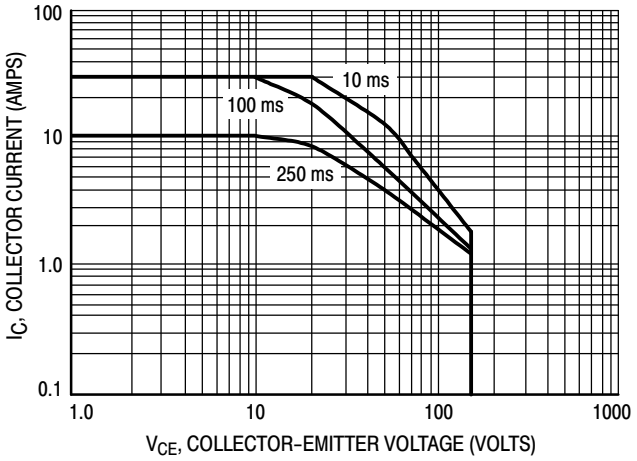


Figure 3. NPN — MJW21192 Safe Operating Area

PNP — MJW21191

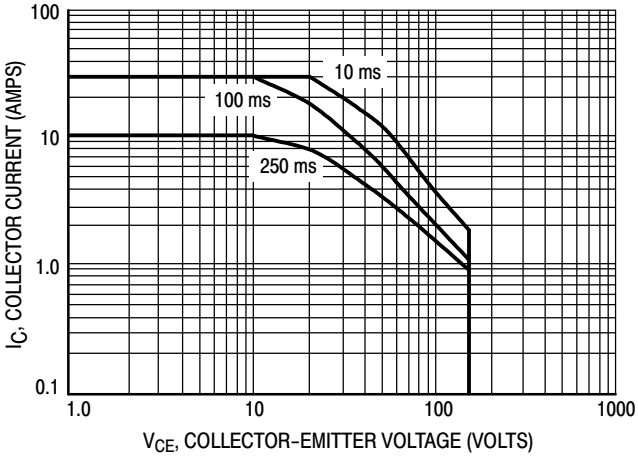


Figure 4. PNP — MJW21191 Safe Operating Area

TYPICAL CHARACTERISTICS

NPN — MJW21192

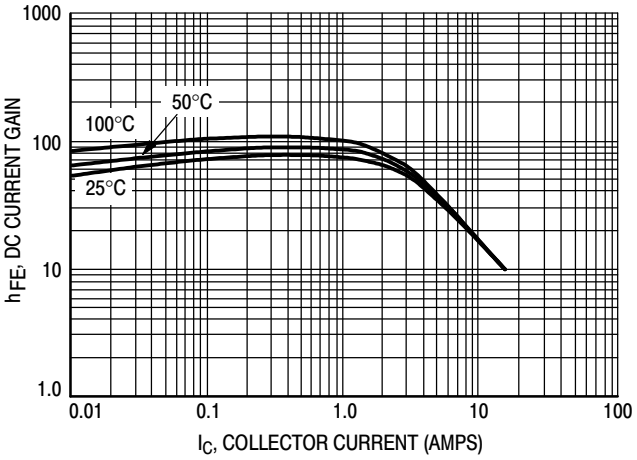


Figure 5. NPN — MJW21192 V_{CE} = 2.0 V DC Current Gain

PNP — MJW21191

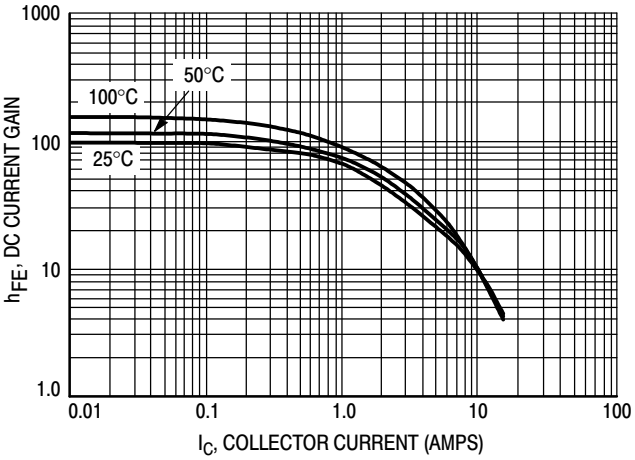


Figure 6. PNP — MJW21191 V_{CE} = 2.0 V DC Current Gain

NPN — MJW21192

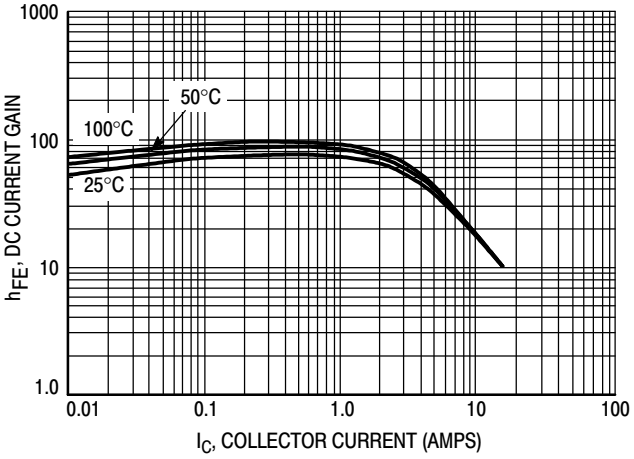


Figure 7. NPN — MJW21192
V_{CE} = 5.0 V DC Current Gain

PNP — MJW21191

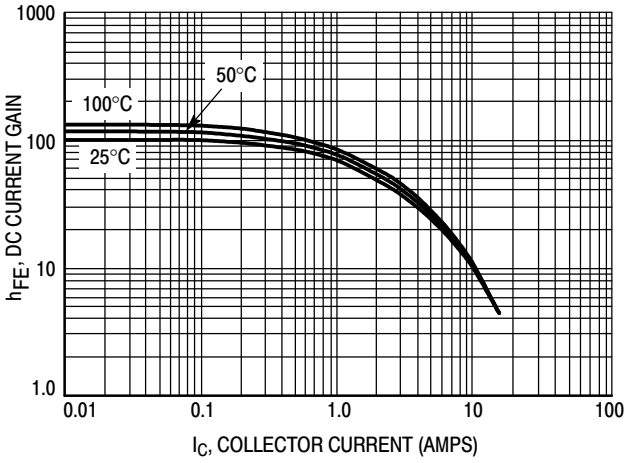


Figure 8. PNP — MJW21191
V_{CE} = 5.0 V DC Current Gain

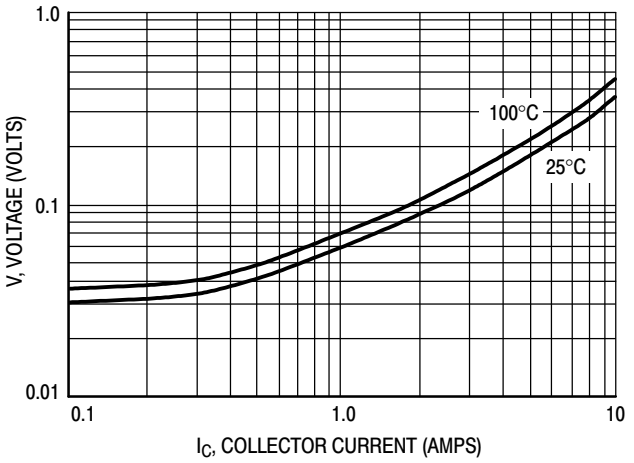


Figure 9. NPN — MJW21192
$V_{CE(sat)}$ I_C/I_B = 5.0

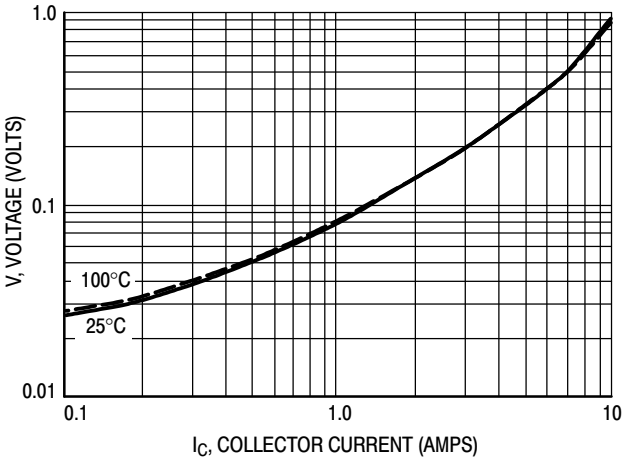


Figure 10. PNP — MJW21191
$V_{CE(sat)}$ I_C/I_B = 5.0

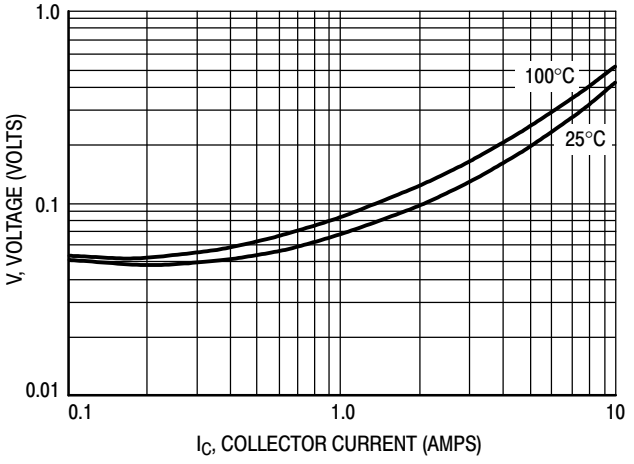


Figure 11. NPN — MJW21192
$V_{CE(sat)}$ I_C/I_B = 10

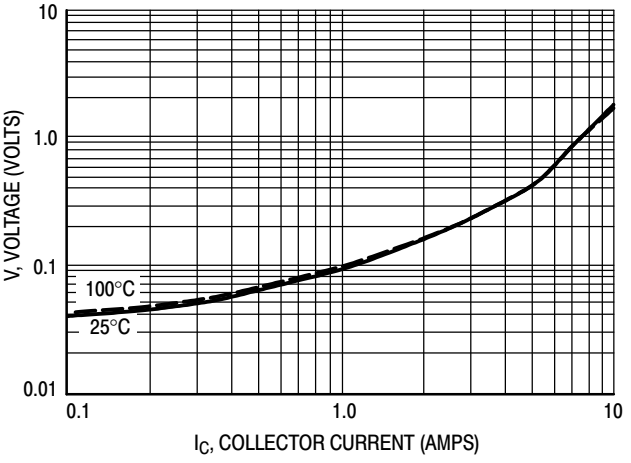


Figure 12. PNP — MJW21191
$V_{CE(sat)}$ I_C/I_B = 10

NPN — MJW21192

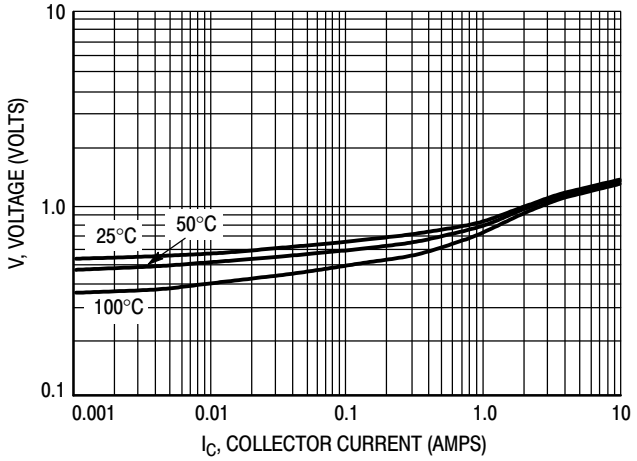


Figure 13. NPN — MJW21192
V_{CE} = 2.0 V $V_{BE(on)}$ Curve

PNP — MJW21191

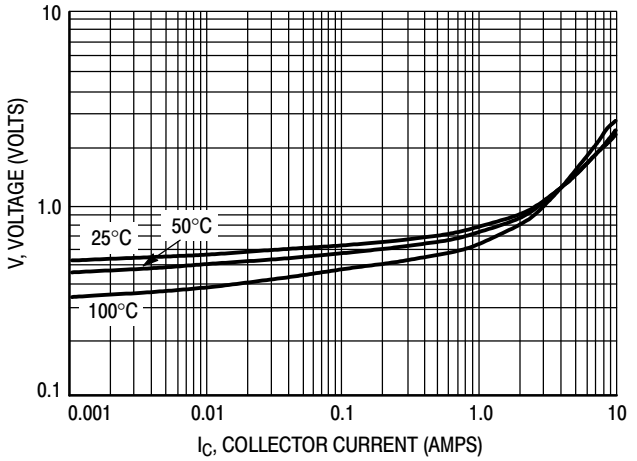


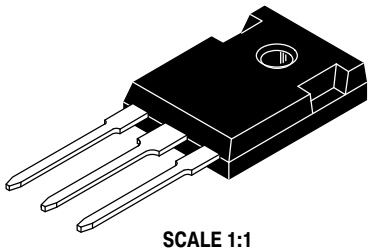
Figure 14. PNP — MJW21191
V_{CE} = 2.0 V $V_{BE(on)}$ Curve

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

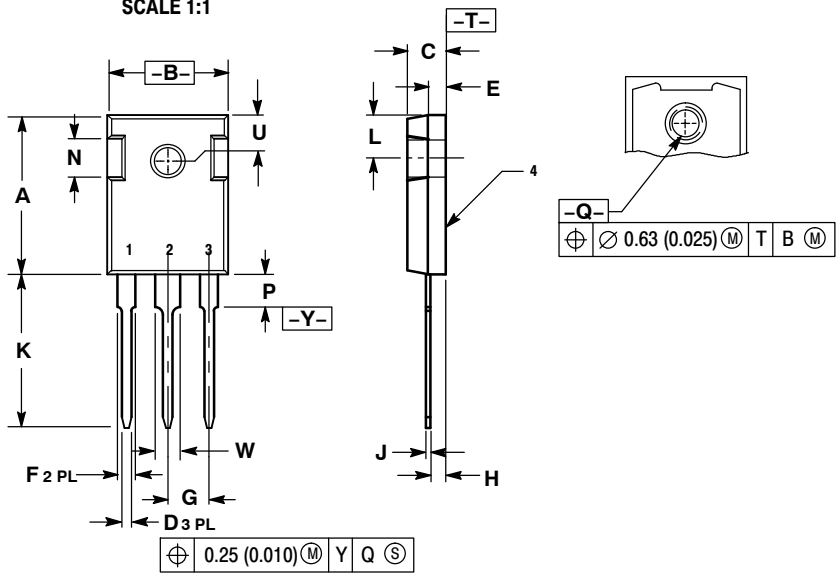
ON Semiconductor®

TO−247
CASE 340L−02
ISSUE F

DATE 26 OCT 2011



SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	20.32	21.08	0.800	8.30
B	15.75	16.26	0.620	0.640
C	4.70	5.30	0.185	0.209
D	1.00	1.40	0.040	0.055
E	1.90	2.60	0.075	0.102
F	1.65	2.13	0.065	0.084
G	5.45 BSC		0.215 BSC	
H	1.50	2.49	0.059	0.098
J	0.40	0.80	0.016	0.031
K	19.81	20.83	0.780	0.820
L	5.40	6.20	0.212	0.244
N	4.32	5.49	0.170	0.216
P	---	4.50	---	0.177
Q	3.55	3.65	0.140	0.144
U	6.15 BSC		0.242 BSC	
W	2.87	3.12	0.113	0.123

STYLE 1:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 2:
PIN 1. ANODE
2. CATHODE (S)
3. ANODE 2
4. CATHODES (S)

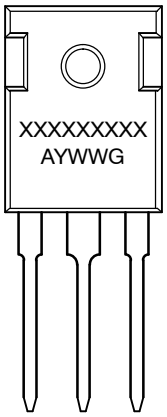
STYLE 3:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 6:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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NEW STANDARD:		
DESCRIPTION:	TO−247	PAGE 1 OF 2

ISSUE	REVISION	DATE
D	CHANGE OF OWNERSHIP FROM MOTOROLA TO ON SEMICONDUCTOR. DIM A WAS 20.80–21.46/0.819–0.845. DIM K WAS 19.81–20.32/0.780–0.800. UPDATED STYLE 1, ADDED STYLES 2, 3, & 4. REQ. BY L. HAYES.	25 AUG 2000
E	DIM E MINIMUM WAS 2.20/0.087. DIM K MINIMUM WAS 20.06/0.790. ADDED GENERIC MARKING DIAGRAM. REQ. BY S. ALLEN.	26 FEB 2010
F	ADDED STYLES 5 AND 6. REQ. BY J. PEREZ.	26 OCT 2011

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