μPD41256
262,144 x 1-Bit
Dynamic NMOS RAM

Description

The μPD41256 is a 262,144-word by 1-bit dynamic RAM designed to operate from a single +5-volt power supply and fabricated with a double polylayer, N-channel, silicon-gate process for high density, high performance, and high reliability. A single-transistor storage cell and advanced dynamic circuitry, including 1024 sense amplifiers, ensure that power dissipation is minimized, while an on-chip circuit generates the negative-voltage substrate bias—automatically and transparently.

The three-state output is controlled by $\overline{CAS}$ independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is held on the output by holding $\overline{CAS}$ low. The data output is returned to high impedance by returning $\overline{CAS}$ high. A hidden refresh feature allows $\overline{CAS}$ to be held low to maintain output data while $\overline{RAS}$ is used to execute refresh cycles.

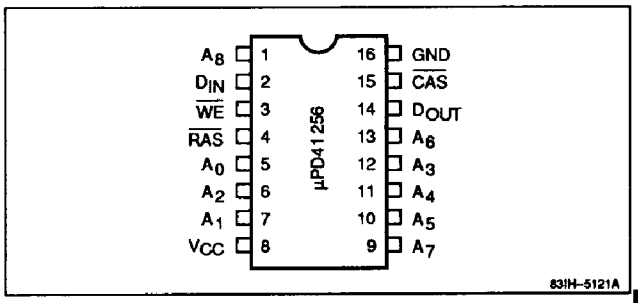
Refreshing may be accomplished by means of $\overline{RAS}$-only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or by normal read or write cycles on the 256 address combinations of A_0 through A_7 during a 4-ms refresh period.

Features

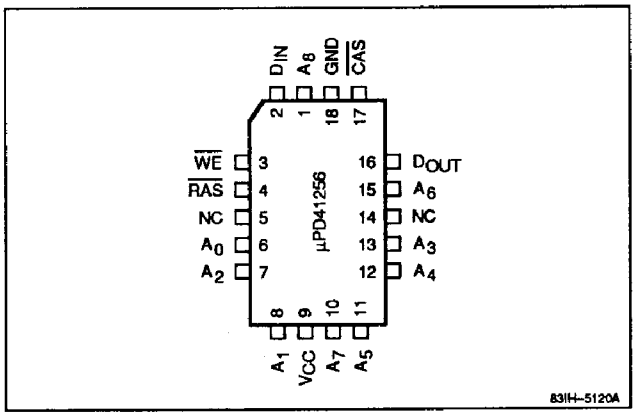
- 262,144-word x 1-bit organization
- High-density plastic DIP and PLCC packaging
- Multiplexed address inputs
- Single +5-volt power supply
- On-chip substrate bias generator
- Low power dissipation of 28 mW max (standby)
- Nonlatched, three-state outputs
- Fully TTL-compatible inputs and outputs
- Low input capacitance
- 256 refresh cycles every 4 ms
- Optional page cycle
- $\overline{RAS}$-only, hidden, and $\overline{CAS}$ before $\overline{RAS}$ refreshing

Pin Configurations

16-Pin Plastic DIP



18-Pin Plastic Leaded Chip Carrier (PLCC)



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Ordering Information

Part Number	Row Access Time (max)	R/W Cycle (min)	Page Cycle (min)	Power Supply Tolerance	Package
μPD41256C-80	80 ns	160 ns	70 ns	±5%	16-pin plastic DIP
C-85	85 ns	165 ns	70 ns		
C-10	100 ns	200 ns	100 ns	±10%	
μPD41256L-80	80 ns	160 ns	70 ns	±5%	18-pin plastic leaded chip carrier
L-85	85 ns	165 ns	70 ns		
L-10	100 ns	200 ns	100 ns	±10%	

Pin Identification

Name	Function
A_0 - A_8	Address inputs
$\overline{CAS}$	Column address strobe
D_{IN}	Data input
D_{OUT}	Data output
$\overline{RAS}$	Row address strobe
$\overline{WE}$	Write enable
GND	Ground
V_{CC}	+5-volt power supply
NC	No connection

Capacitance

T_A = 25°C; f = 1 MHz

Parameter	Symbol	Max	Unit	Pins Under Test
Input capacitance	C_{I1}	5	pF	A_0 - A_8, D_{IN}
	C_{I2}	8	pF	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$
Output capacitance	C_{OUT}	7	pF	D_{OUT}

Absolute Maximum Ratings

Voltage on any pin relative to GND, V_T	−1.0 to +7.0 V
Operating temperature, T_A (ambient)	0 to +70°C
Storage temperature, T_{STG}	−55 to +125°C
Short-circuit output current, I_{OS}	50 mA
Power dissipation, P_D	1.0 W

Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The device should be operated within the limits specified under DC and AC Characteristics.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage, high	V_{IH}	2.4		V_{CC} + 1.0	V
Input voltage, low	V_{IL}	−1.0		0.8	V
Ambient temperature	T_A	0		70	°C

Notes:

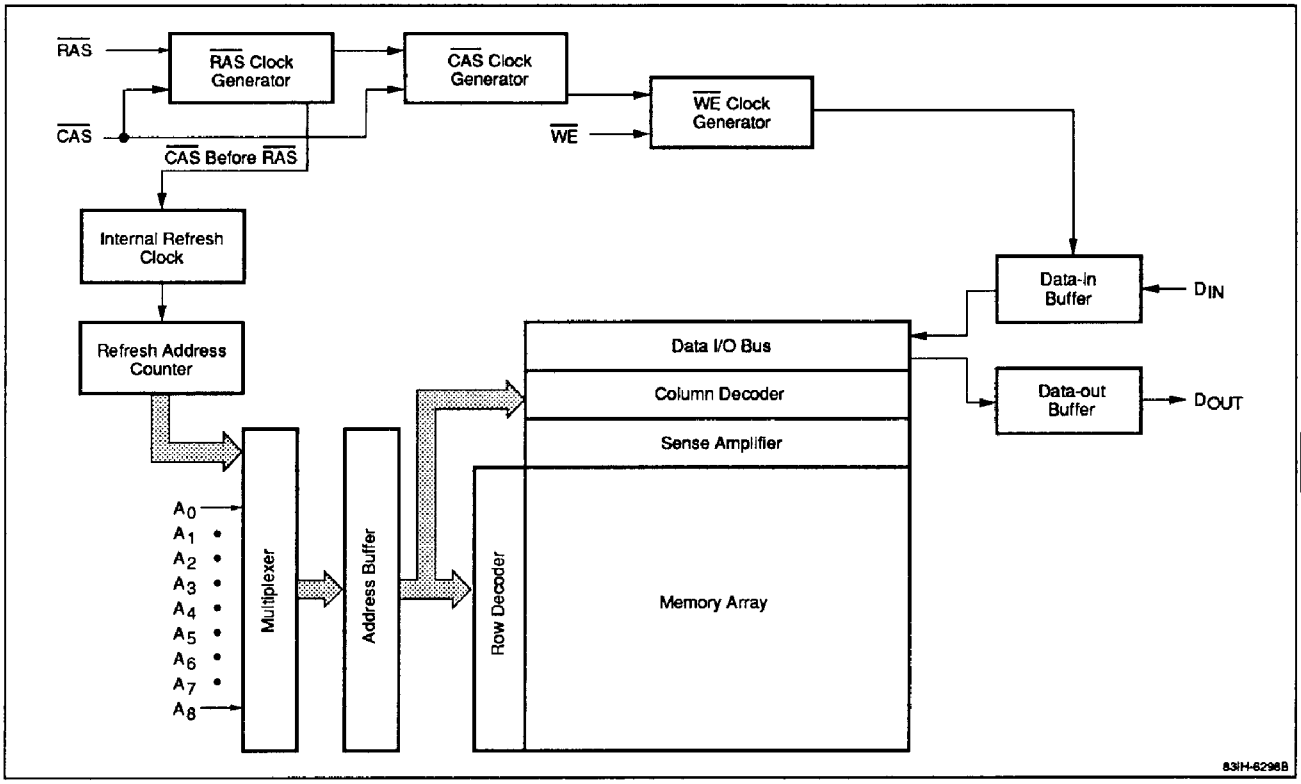
(1) V_{CC} = +5 V ±5% for the −80 and −85 versions.

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5.0 V ±10%

Parameter	Symbol	Min	Max	Unit	Test Conditions
Standby supply current	I_{CC2}		5.0	mA	$\overline{RAS}$ = V_{IH}; D_{OUT} = high impedance
Input leakage current	$I_{I(L)}$	−10	10	μA	V_{IN} = 0 V to V_{CC}; all other pins not under test = 0 V
Output leakage current	$I_{O(L)}$	−10	10	μA	D_{OUT} disabled; V_{OUT} = 0 V to V_{CC}
Output voltage, low	V_{OL}		0.4	V	I_{OL} = 4.2 mA
Output voltage, high	V_{OH}	2.4		V	I_{OUT} = −5 mA

Block Diagram



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AC Characteristics

T_A = 0 to +70°C

Parameter	Symbol	μPD41256-80 Min	μPD41256-80 Max	μPD41256-85 Min	μPD41256-85 Max	μPD41256-10 Min	μPD41256-10 Max	Unit	Test Conditions
Supply voltage	V_{CC}	4.75	5.25	4.75	5.25	4.5	5.5		
Operating supply current, average	I_{CC1}		90		90		80	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; $t_{RC} = t_{RC}$ (min); I_O = 0 mA (Note 5)
Operating supply current, $\overline{RAS}$-only refresh cycle, average	I_{CC3}		80		80		65	mA	$\overline{RAS}$ cycling; $\overline{CAS} \geq V_{IH}$; $t_{RC} = t_{RC}$ (min); I_O = 0 mA (Note 5)
Operating supply current, page cycle, average	I_{CC4}		70		70		60	mA	$\overline{RAS} \leq V_{IL}$; $\overline{CAS}$ cycling; $t_{PC} = t_{PC}$ (min); I_O = 0 mA (Note 5)
Operating current, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, average	I_{CC5}		80		80		65	mA	$\overline{CAS} \leq V_{IL}$; $\overline{RAS}$ cycling; $t_{RC} = t_{RC}$ (min); I/O = 0 mA (Note 5)
Random read or write cycle time	t_{RC}	180		165		200		ns	(Note 6)
Read-write cycle time	t_{RWC}	185		195		240		ns	(Note 6)
Page cycle time	t_{PC}	70		70		100		ns	(Note 6)
Access time from $\overline{RAS}$	t_{RAC}		80		85		100	ns	(Notes 7, 8)
Access time from $\overline{CAS}$	t_{CAC}		40		40		50	ns	(Notes 7, 9)

AC Characteristics (cont)

Parameter	Symbol	μPD41256-80 Min	μPD41256-80 Max	μPD41256-85 Min	μPD41256-85 Max	μPD41256-10 Min	μPD41256-10 Max	Unit	Test Conditions
Output buffer turnoff delay	t_{OFF}	0	20	0	20	0	25	ns	(Note 10)
Rise and fall transition time	t_T	3	50	3	50	3	50	ns	(Note 4)
$\overline{RAS}$ precharge time	t_{RP}	70		70		90		ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	16,000	85	16,000	100	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	40		40		50		ns	
$\overline{CAS}$ pulse width	t_{CAS}	40	10,000	40	10,000	50	10,000	ns	
$\overline{CAS}$ hold time	t_{CSH}	80		85		100		ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	40	20	45	20	50	ns	(Note 11)
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10		10		10		ns	(Note 12)
$\overline{CAS}$ precharge time, nonpage cycle	t_{CPN}	25		25		25		ns	
$\overline{CAS}$ precharge time, page cycle	t_{CP}	20		20		40		ns	
$\overline{RAS}$ precharge $\overline{CAS}$ hold time	t_{RPC}	0		0		0		ns	
Row address setup time	t_{ASR}	0		0		0		ns	
Row address hold time	t_{RAH}	10		10		10		ns	
Column address setup time	t_{ASC}	0		0		0		ns	
Column address hold time	t_{CAH}	15		20		15		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	55		65		65		ns	
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time referenced to $\overline{RAS}$	t_{RRH}	10		10		10		ns	(Note 13)
Read command hold time referenced to $\overline{CAS}$	t_{RCH}	0		0		0		ns	(Note 13)
Write command hold time	t_{WCH}	20		20		25		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	60		65		75		ns	
Write command pulse width	t_{WP}	20		15		15		ns	(Note 17)
Write command to $\overline{RAS}$ lead time	t_{RWL}	20		30		35		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	20		30		35		ns	
Data-in setup time	t_{DS}	0		0		0		ns	(Note 14)
Data-in hold time	t_{DH}	20		20		25		ns	(Note 14)
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	60		65		75		ns	
Refresh period	t_{REF}		4		4		4	ms	Addresses A_0 - A_7
$\overline{WE}$ command setup time	t_{WCS}	0		0		0		ns	(Note 15)
$\overline{CAS}$ to $\overline{WE}$ delay	t_{CWD}	40		40		50		ns	(Note 15)
$\overline{RAS}$ to $\overline{WE}$ delay	t_{RWD}	80		85		100		ns	(Note 15)
$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CSR}	10		10		10		ns	(Note 16)

AC Characteristics (cont)

Parameter	Symbol	μPD41256-80 Min	μPD41256-80 Max	μPD41256-85 Min	μPD41256-85 Max	μPD41256-10 Min	μPD41256-10 Max	Unit	Test Conditions
$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh cycle	t_{CHR}	20		15		20		ns	(Note 16)
Read-write cycle time (counter test cycle)	t_{TRC}	N/A		N/A		220		ns	(Note 18)
Read-write cycle time (counter test cycle)	t_{TRWC}	N/A		N/A		260		ns	(Note 18)

Notes:

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-up, followed by any eight $\overline{RAS}$ cycles, before proper device operation is achieved.

(3) AC measurements assume t_T = 5 ns.

(4) V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

(5) I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open.

(6) The minimum specifications are used only to indicate the cycle time at which proper operation over the full temperature range (T_A = 0 to +70°C) is assured.

(7) Output load = 2 TTL loads and 100 pF

(8) Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

(9) Assumes that $t_{RCD} \geq t_{RCD}$ (max)

(10) t_{OFF} (max) defines the time at which the output achieves the open-circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the t_{RCD} (max) limit assures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.

(12) The t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycle.

(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) These parameters are referenced to the leading edge of $\overline{CAS}$ in early write cycles and to the leading edge of $\overline{WE}$ in delayed write or read-modify-write cycles.

(15) t_{WCS}, t_{CWD}, and t_{RWD} are restrictive operating parameters in read-write and read-modify-write cycles only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data output will remain open-circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the condition of the data output (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.

(16) DIP products with process codes E, K, P and X do not have the $\overline{CAS}$ before $\overline{RAS}$ refresh feature. All other package types and process codes do have $\overline{CAS}$ before $\overline{RAS}$ refreshing.

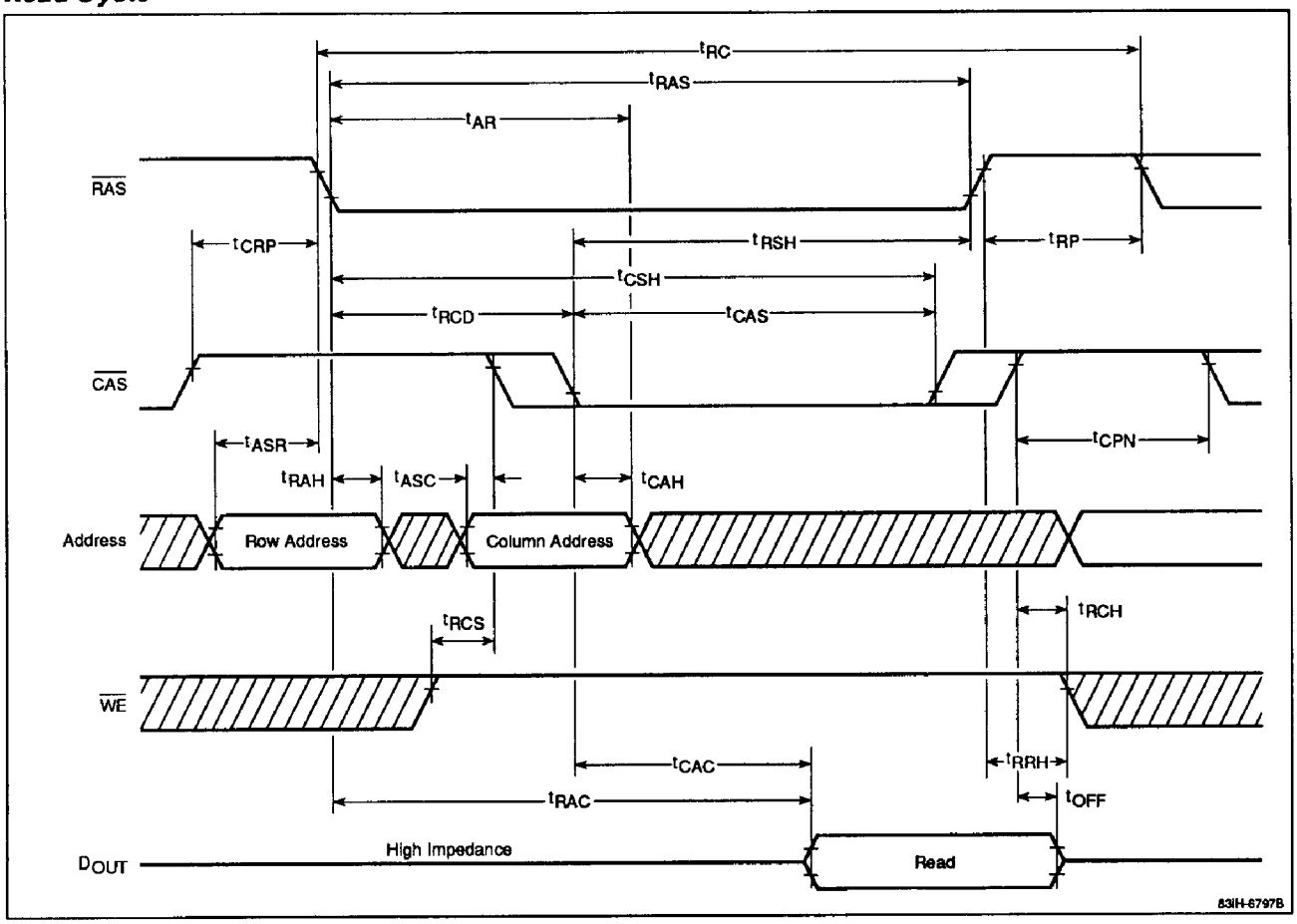
On DIP products with process codes E, K, P and X, the external address inputs are required in hidden refresh cycles and the address timing must satisfy t_{ASR} and t_{RAH}, which are specified with respect to the falling edge of $\overline{RAS}$.

(17) t_{WP} is applicable for a delayed write cycle. If the cycle is early write, it should be satisfied with the specified value of t_{WCH}.

(18) t_{TRC} and t_{TRWL} are applicable for a $\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle.

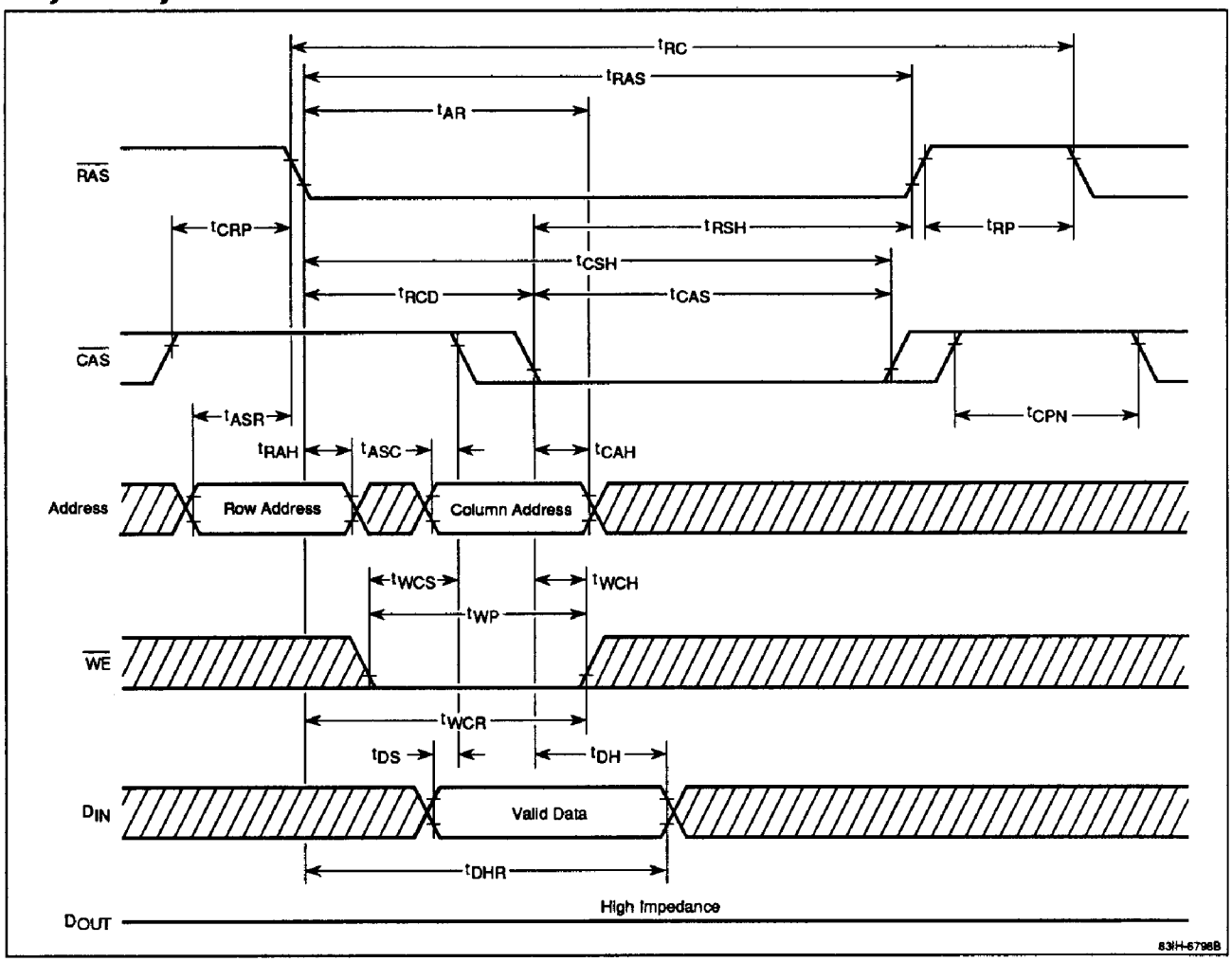
Timing Waveforms

Read Cycle



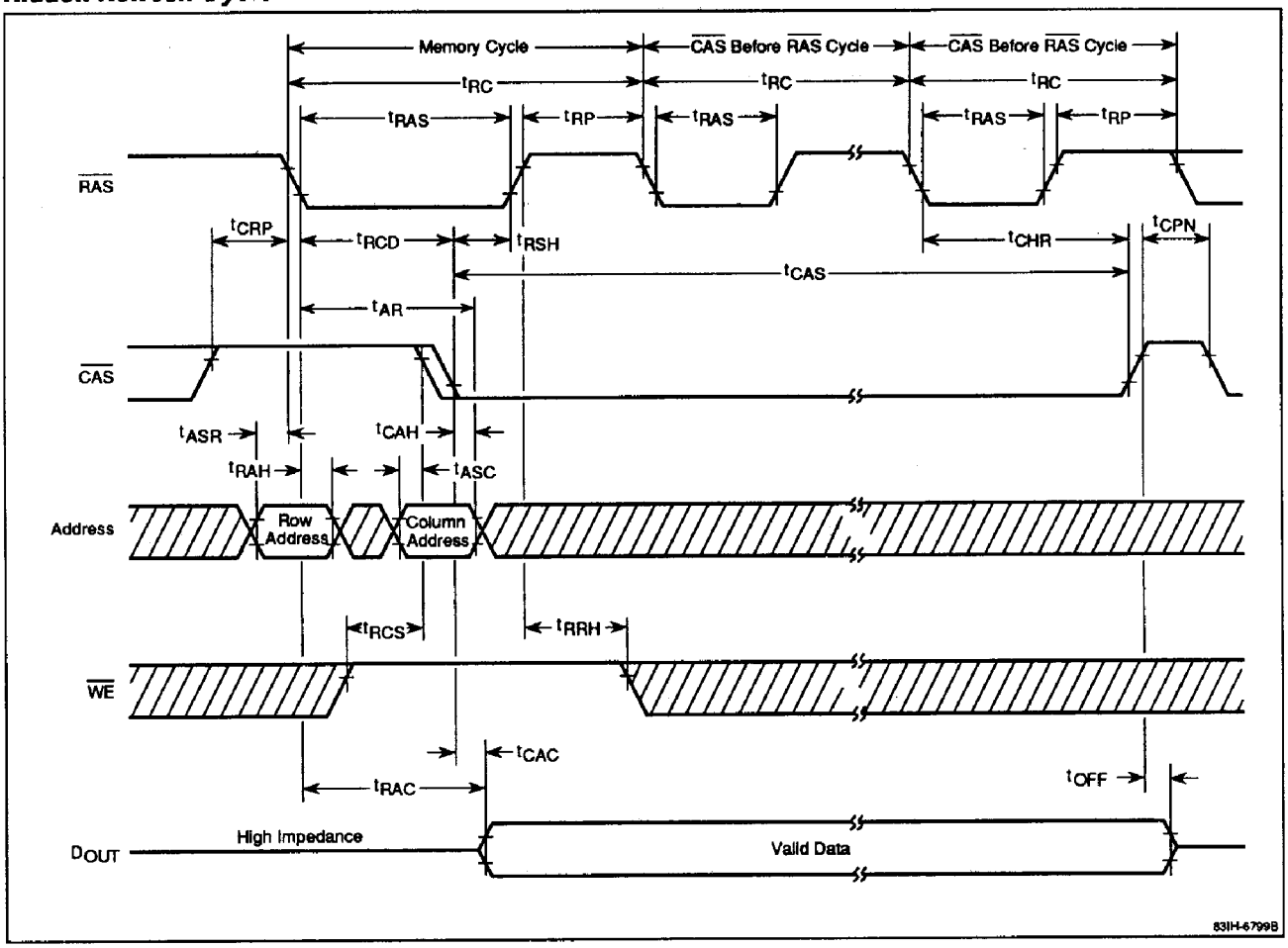
Timing Waveforms (cont)

Early Write Cycle



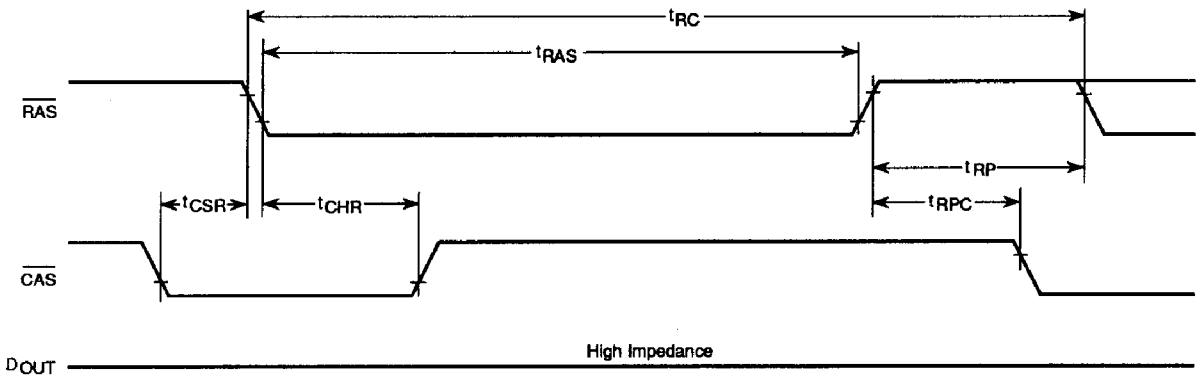
Timing Waveforms (cont)

Hidden Refresh Cycle



Timing Waveforms (cont)

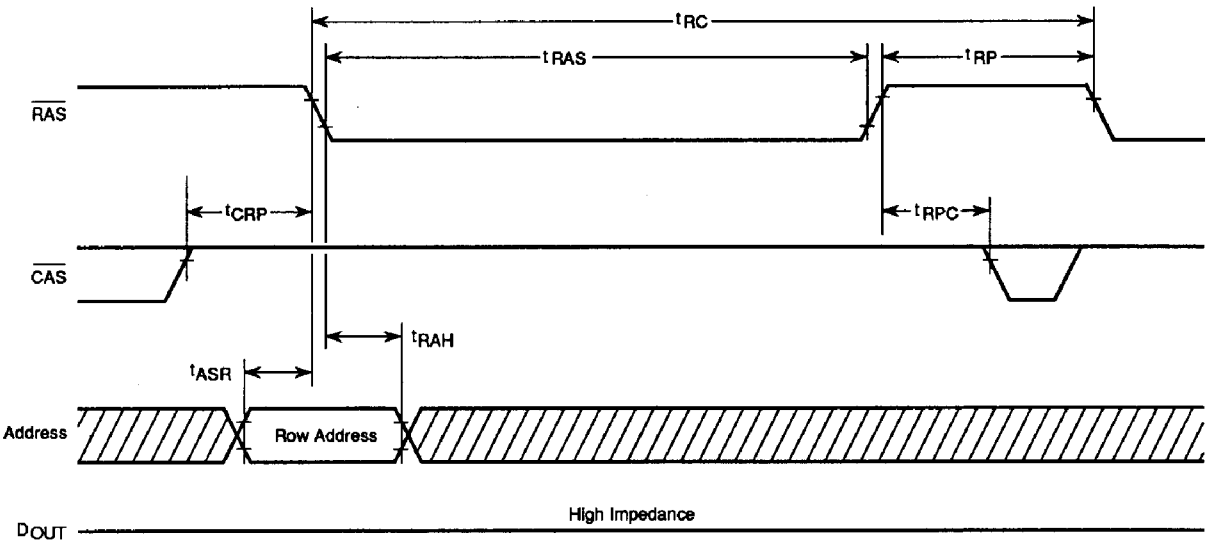
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



Note:
[1] $\overline{WE}$ and Address = don't care.

83IH-6592B

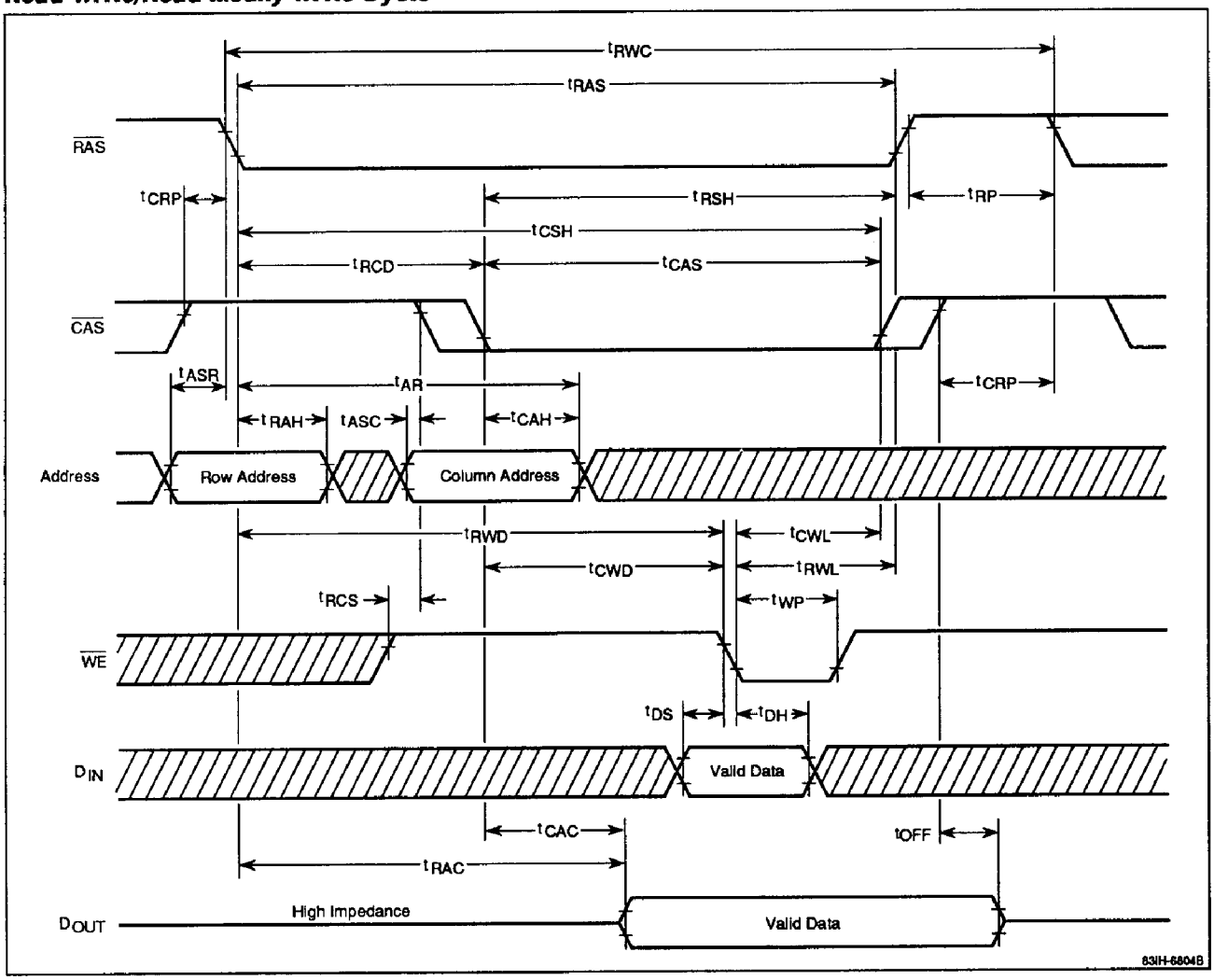
$\overline{RAS}$-Only Refresh Cycle



83IH-6594B

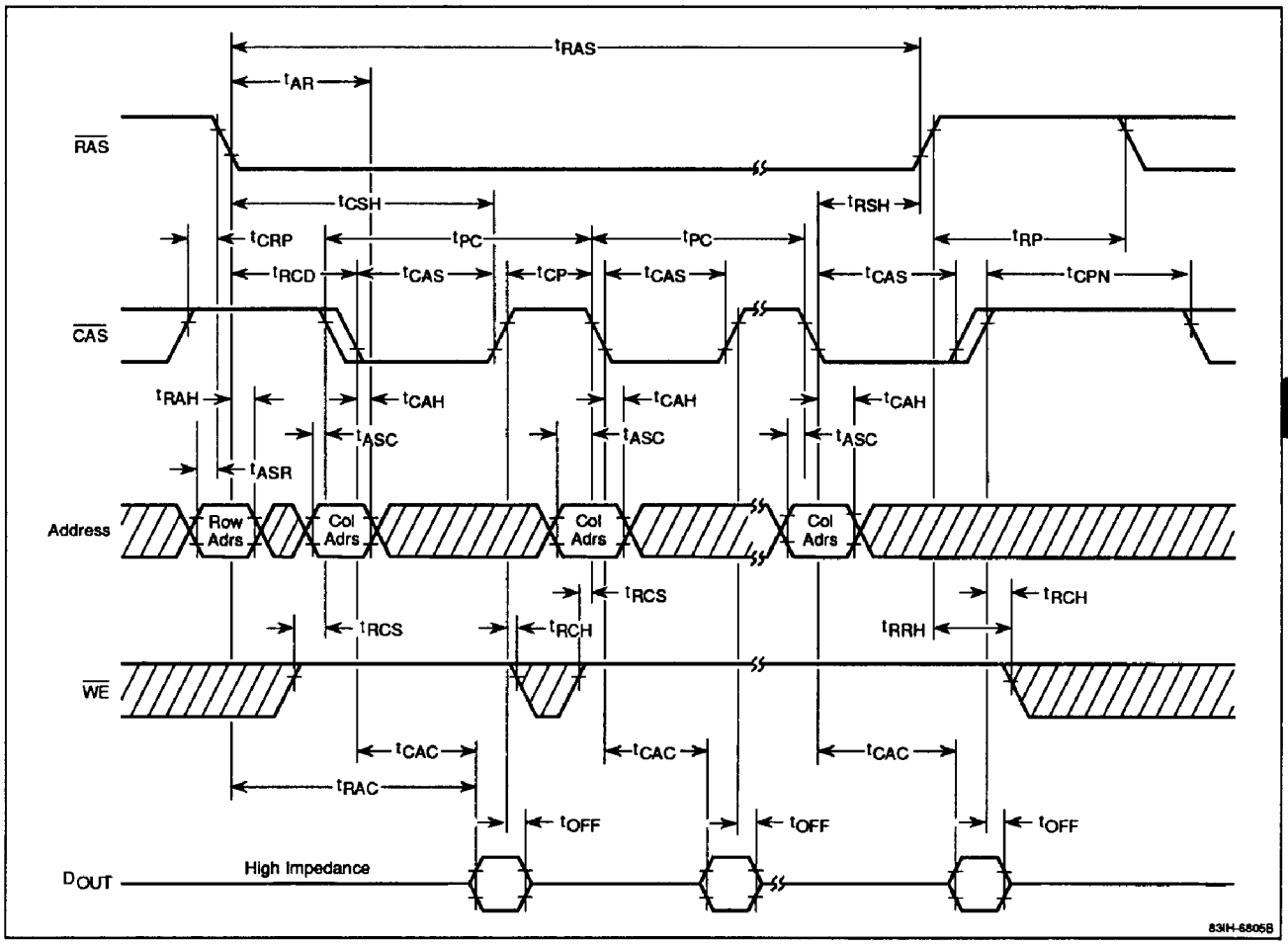
Timing Waveforms (cont)

Read-Write/Read-Modify-Write Cycle



Timing Waveforms (cont)

Page Read Cycle



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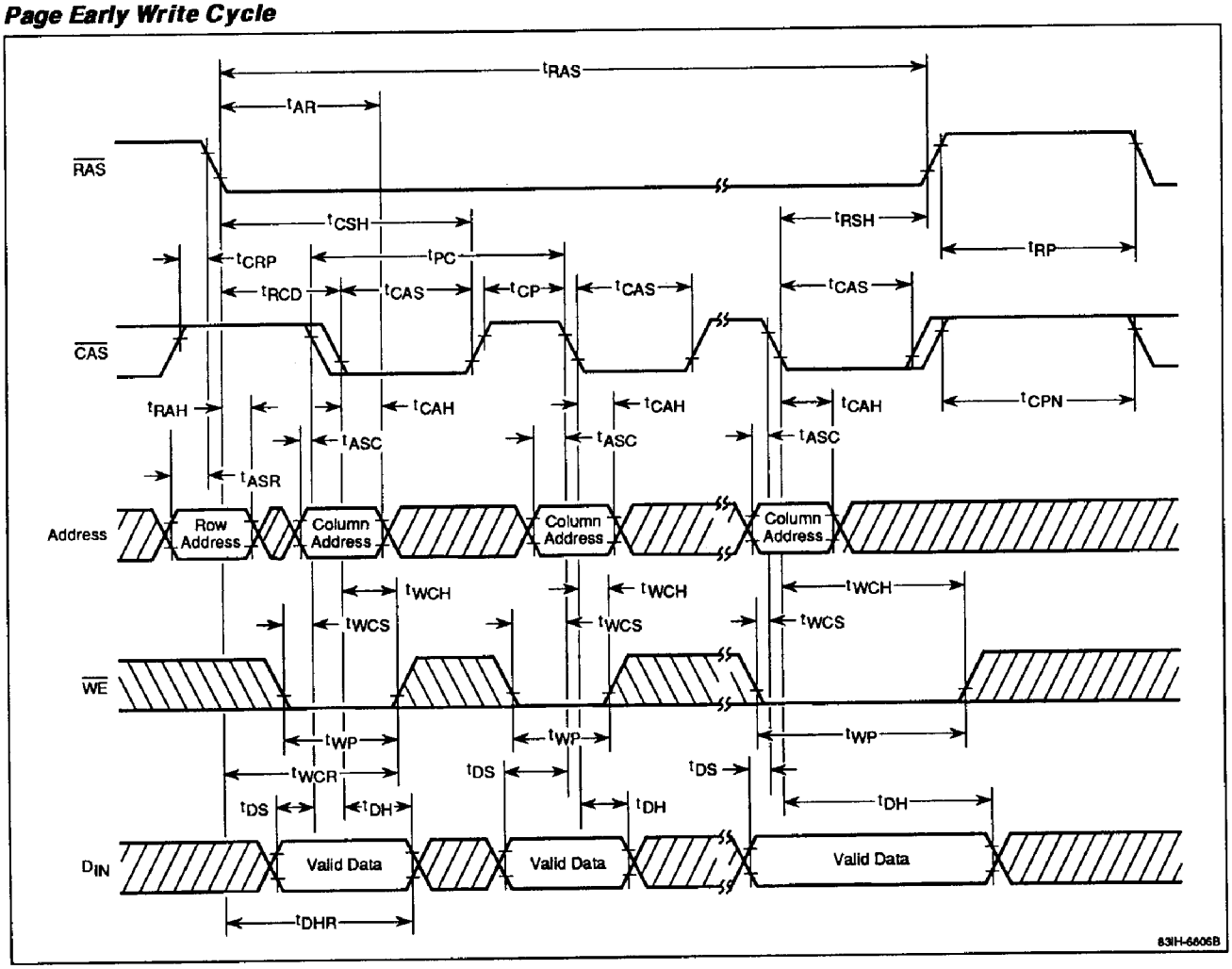
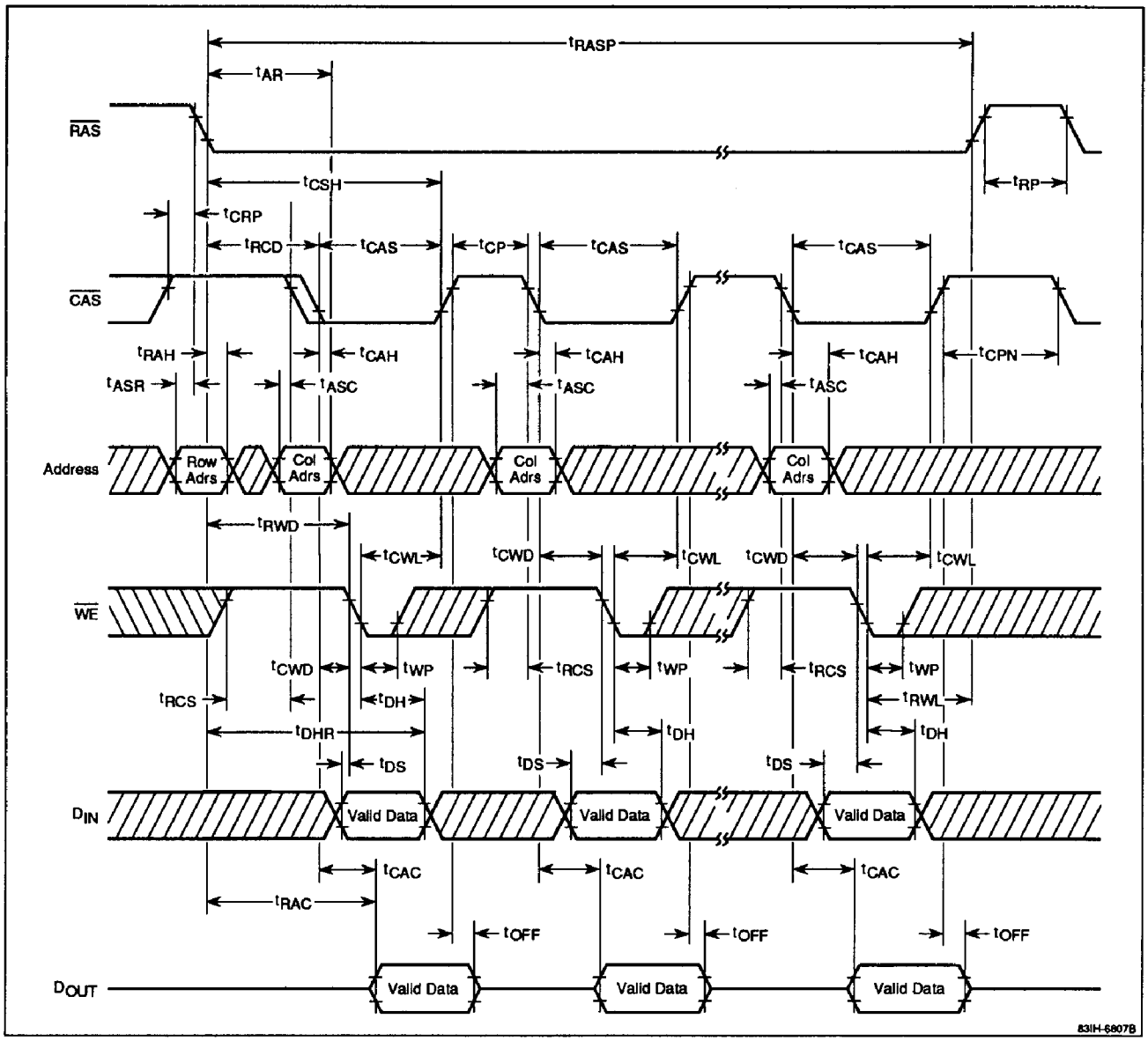
Timing Waveforms (cont)

Page Early Write Cycle



Timing Waveforms (cont)

Page Read-Write/Read-Modify-Write Cycle



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$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test

The μPD41256 provides a method to verify proper operation of the internal address counter used in $\overline{CAS}$ before $\overline{RAS}$ refreshing. After a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle is initiated, $\overline{CAS}$ satisfies a hold time (t_{CHR}), a precharge time (t_{CP}), and then returns low while $\overline{RAS}$ is held low to enable read, write, or read-modify-write operation. As shown in the appropriate timing waveforms, a refresh counter test can be initiated at this point on specified row and column addresses. The row is selected by the internal address counter, and the column is defined by an external address supplied at the second falling edge of $\overline{CAS}$. Test patterns can be generated in several ways; the following example is one possibility. Any pattern must be preceded by the normal power-up procedure containing a pause of 100 μs and then eight $\overline{RAS}$ cycles to initialize the internal counter.

(1) Write "0" into 256 memory cells with 256 $\overline{CAS}$ before $\overline{RAS}$ refresh counter test write cycles. Use the same column address in each cycle.

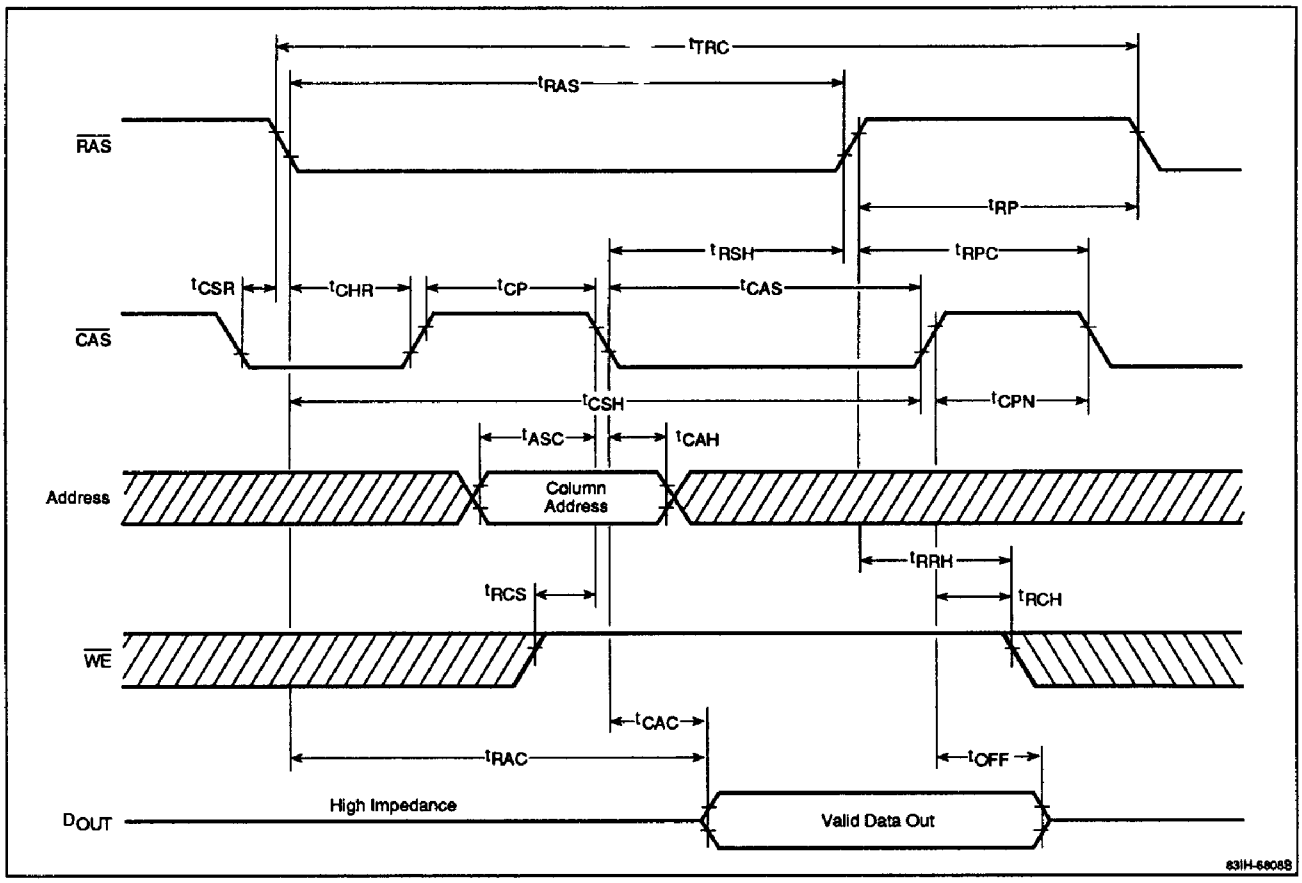
(2) Use a counter test read-modify-write cycle to read the "0" written in the first cycle of step 1 and then write a "1" into that location in the same cycle. Perform this operation 256 times, until a "1" is written into each of the 256 memory cells. Continue using the same column address as specified in step 1.

(3) Read each "1" written in step 2 using a counter test read cycle.

(4) Complement the test pattern and repeat steps 1, 2, and 3.

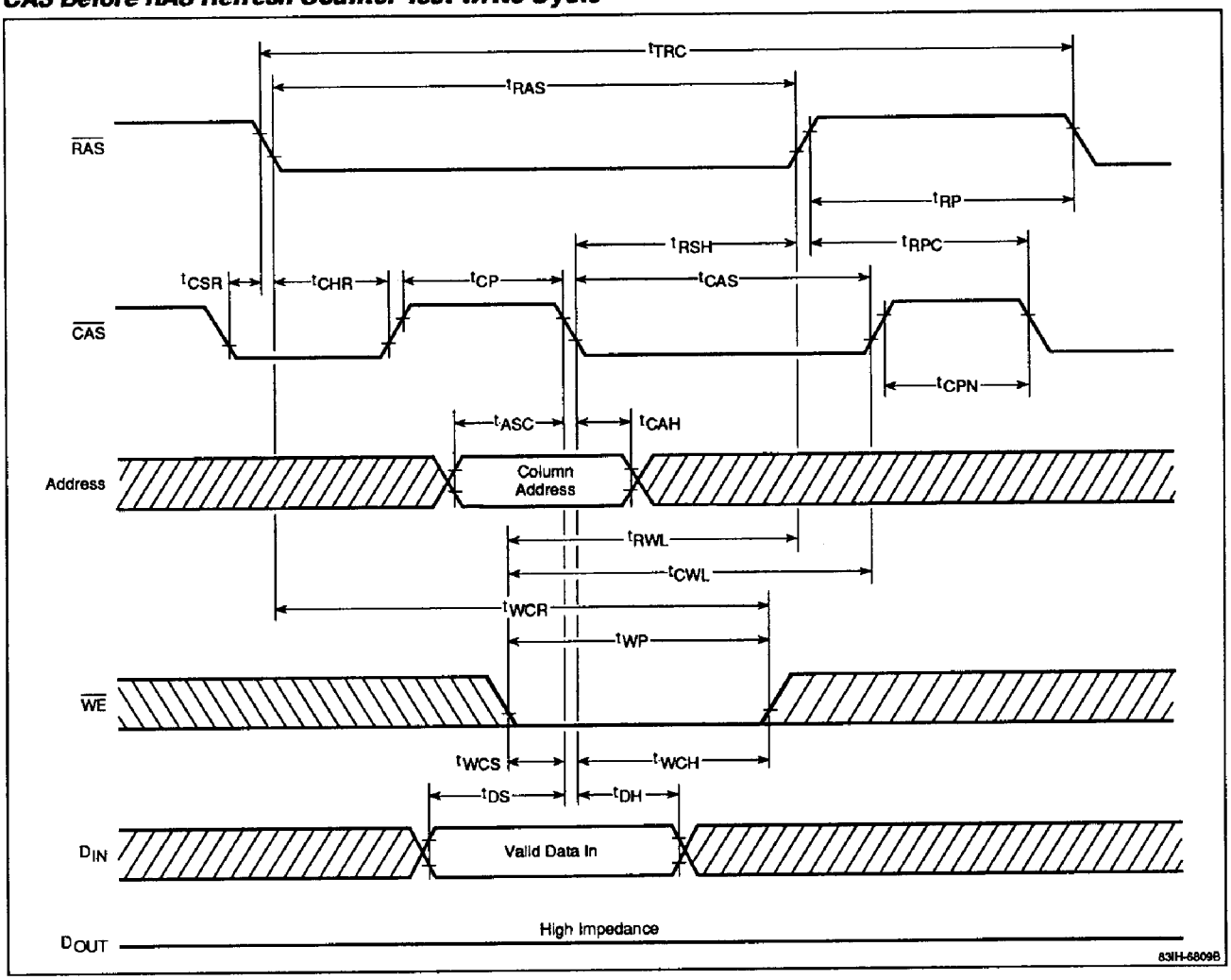
Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Read Cycle



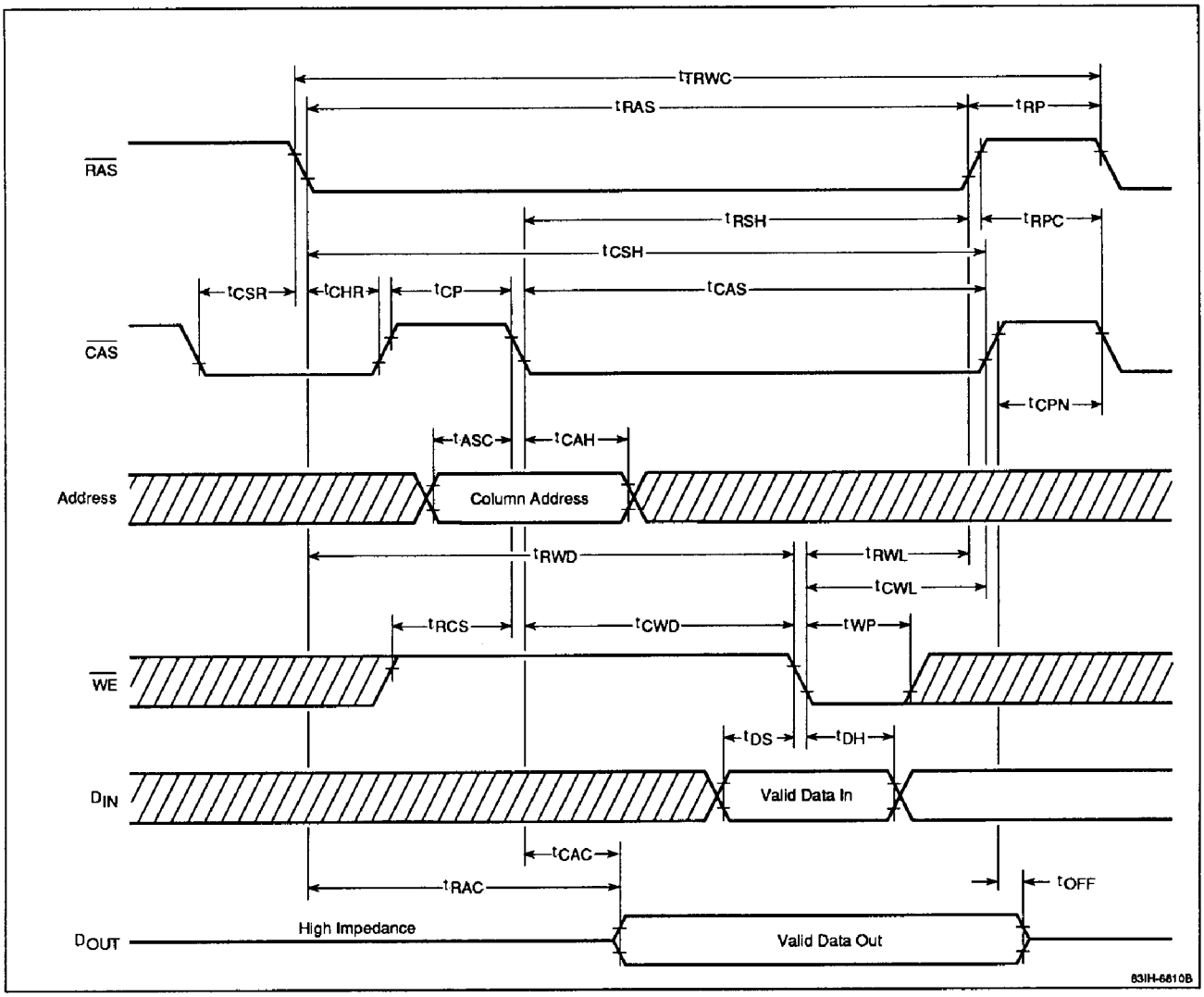
Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Write Cycle



Timing Waveforms (cont)

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Counter Test Read-Modify-Write Cycle



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